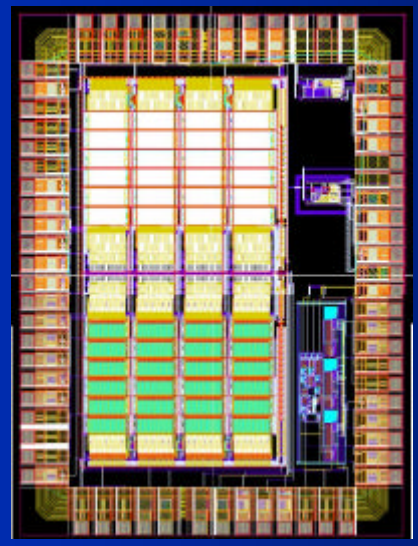
Development of new electronics

Front end for Optical Module



(Km^3 Cherenkov detector)

D. Lo Presti, N. Randazzo, L. Caponetto, L. Lo Nigro

OPTICAL MODULE (OM)

Each optical module is composed by :

- a large area PMT: 8” diameter or greater;
- a mu-metal shield for PMT;
- fast electronics modules for the signal readout and digitization;
- slow electronics modules (slow control) to control the essential parameters of the OM itself (PMT Supply voltages, Board power supply, ...);
- DC-DC converter to power supply the board and the PMT.

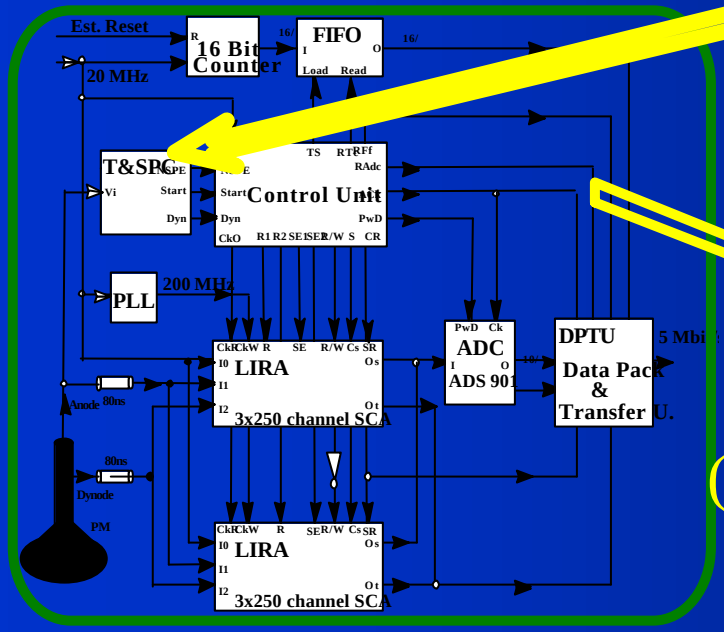
SYSTEM REQUIREMENTS

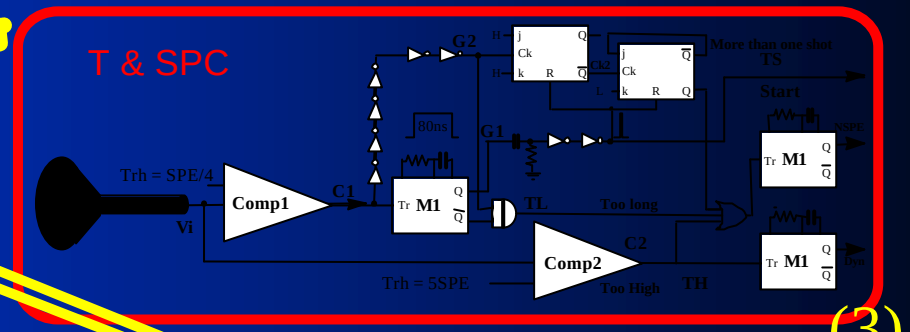
- Very low power because of the distance from the shore;
- Only one submarine interconnecting cable to have the best reliability and to simplify the deployment;
- Flexibility to give the possibility of changing parameters;
- Very small dead-time to get a good detector efficiency;
- High dynamic range to fit with different kinds of experiments;
- Very good accuracy of experimental data;
- Low costs, if possible!

PERFORMANCES

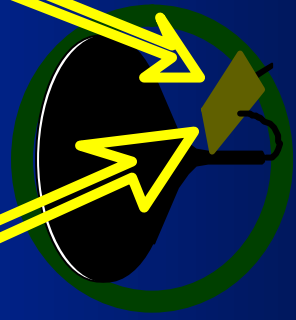
- Not more than 300 mW in each OM;
- Extensive use of full-custom VLSI devices both for analog and digital parts in the OM;
- Power dissipation less than 5 kW (500 mW per module);
- Hardware solution for Trigger;

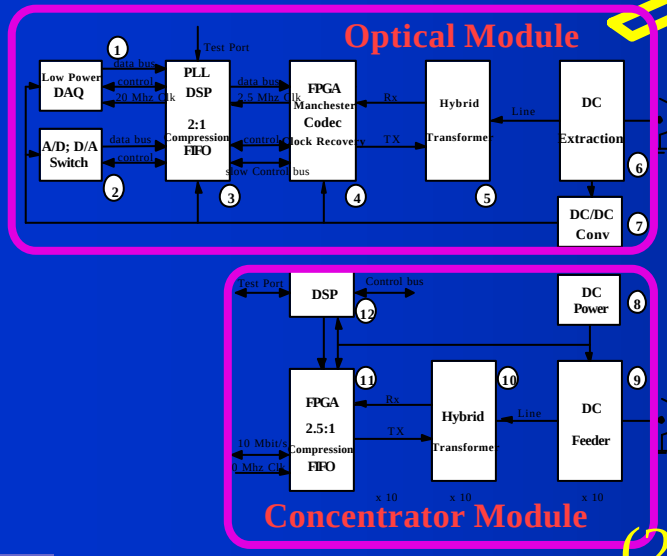
  Software solution for coincidences;
- Dead Time < 0.1%;
- Input dynamic range >14 bit;
- Timing accuracy better than 1 ns.





Optical Module (OM)



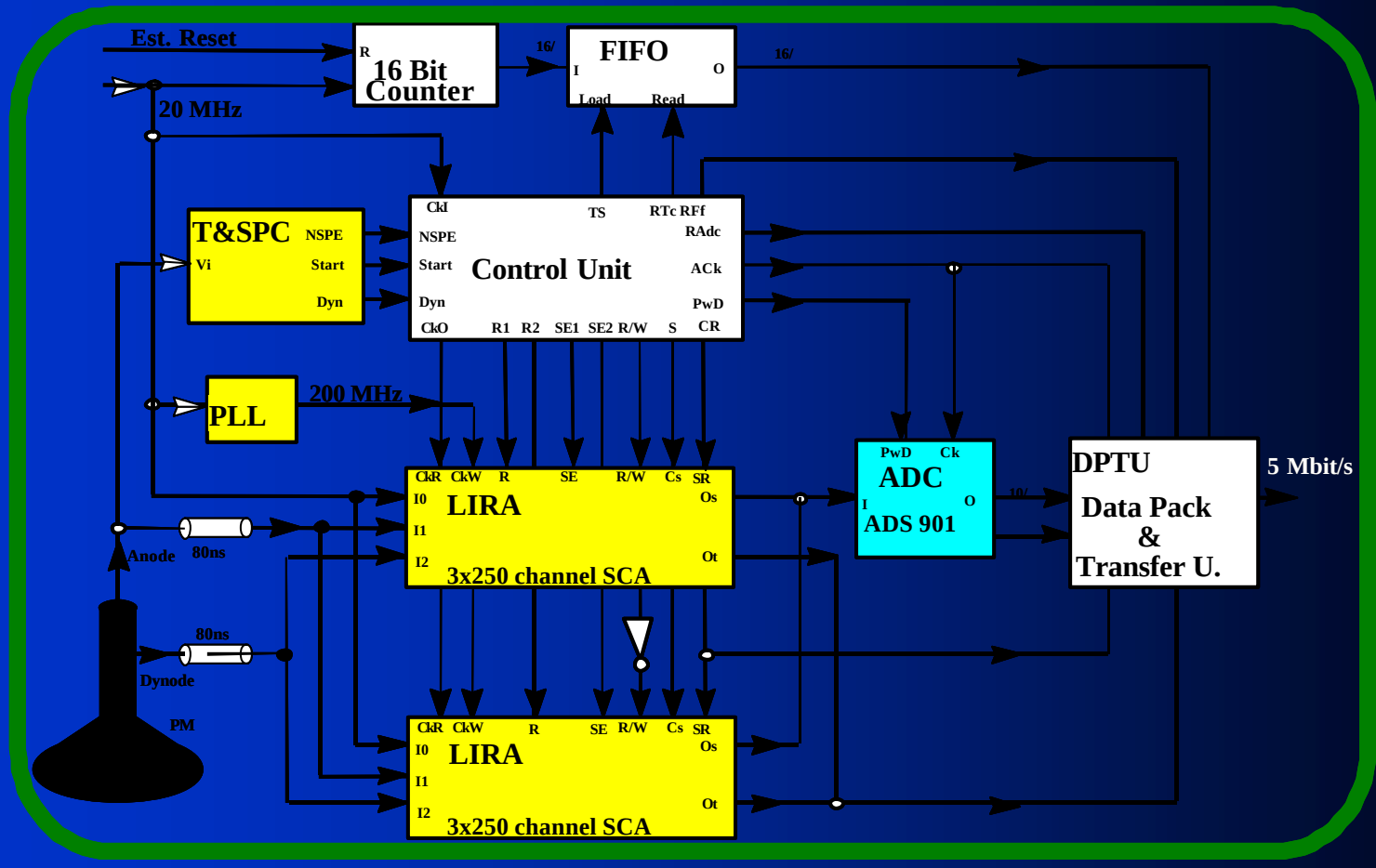


(1) Pre-analysis and storage Unit

(2) Channels concentration & data compression and packaging Unit

(3) Trigger & Single Photon Classifier

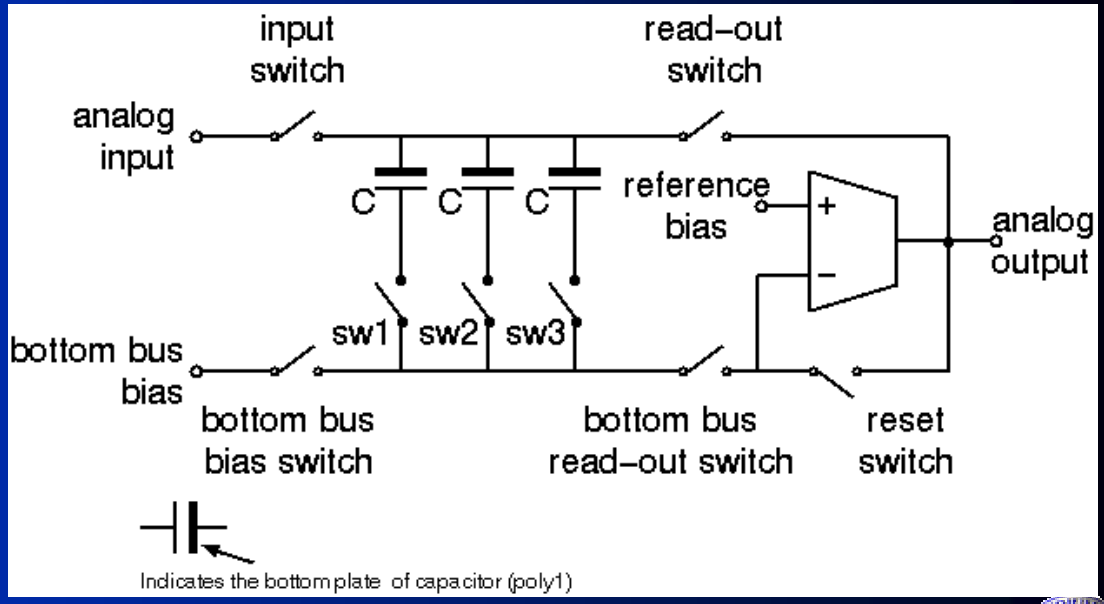
OM FRONT-END Front-end Electronics
VLSI Full custom



on chip on board

Design Specifications of the blocks

- **LIRA**
  - Sampling frequency 200 MHz
  - Readout frequency 10 MHz
  - Resolution ≥ 9 bit
  - Input Dynamic 2 V
  - Input-Output Offset regulation
  - 3 Input
    - Anodo
    - Dinodo
    - Master Clock a 20 MHz
  - 256 cells



Design Specifications of the blocks

- **T&SPC**
  - Trigger unit
  - PMT signals classification
    - 2 thresholds remotely settable by slow control
    - Th1 Trigger SPE/4 → Start signal 5 bit
      - Th2 5 SPE → Dynode samples selection 5 bit
    - Valid Time window NSPE 5 bit
  - Classification time 60 ns remotely settable
- **PLL**
  - Generation of 200 MHz Slave Clock starting from 20 MHz Master Clock
  - I/O frequency ratio adjustable → $V_{control}$

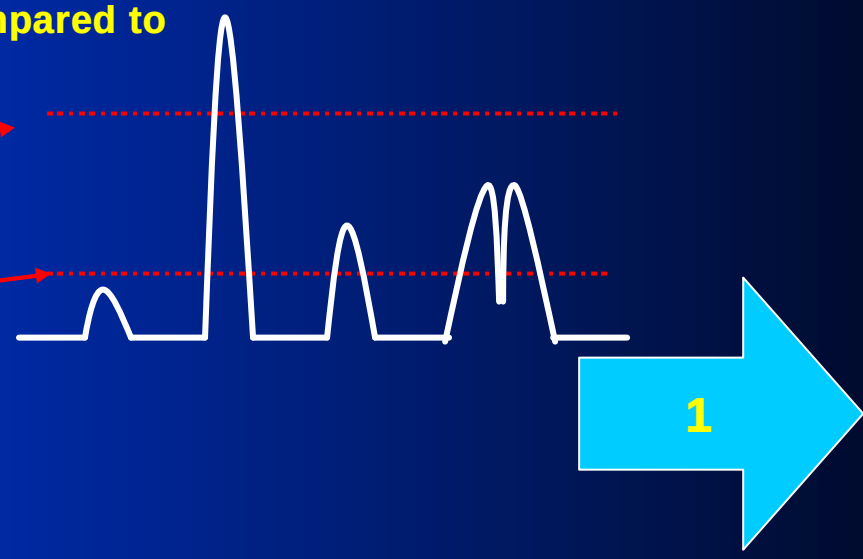
Optical Module Electronics (1)

Working principles

1. The signal coming from the PMT is compared to two Threshold:
   - Th2 = SPEx5 (*):
     - DYN signal.
   - Th1 = SPE/4 (*):
     - START signal;
2. Signal Classification:
   - Delayed START signal
     - ~ 60 ns – Decision Time;
       - More than one hit;
       - Too long (*);
       - Non Single PhotoElectron;

(*) Remotely settable by slow Control:

- DAC 4 bit and latch.



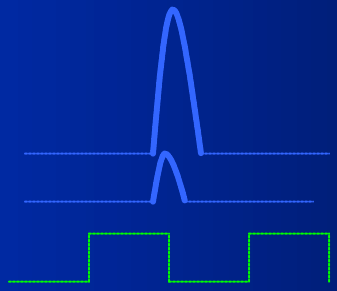
The PMT signal causes a trigger event and after ~ 60 ns it is classified.

The Control Unit receives the start signal and set one of the LIRA in the write phase.

Optical Module Electronics (1)

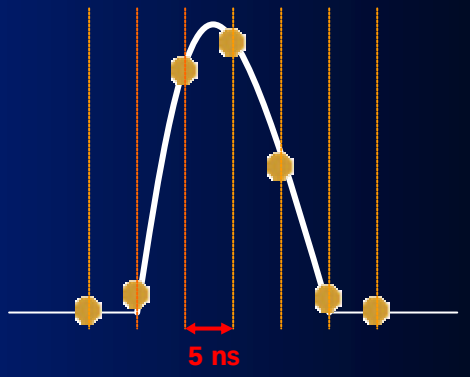
Working principles

1. The Analogue Memory LIRA (256 cells x 3 channels) samples at 200 MHz and transfers the samples at 10 MHz.
2. The 200 MHz clock is produced by PLL starting from 20 MHz Master Clock.
3. Each LIRA samples during write phase:
   - Anode signal;
   - Dynode signal;
   - 20 MHz Master clock.



4. The number of samples is 10 SPE and 100 NSPE (*);
5. Two voltage levels Va e Vb allows offset calibration (*)
6. The 2 LIRA are alternatively in write and read phase.
7. When START signal arrives (Control Unit):
   - One of the LIRA start sampling (10) and if no NSPE signal arrives from TSPC starts reading else continues sampling (100) and then starts reading;
   - The second LIRA waits and only if the first LIRA is full starts its writing phase;

(*) Remotely settable by Slow Control



Scrittura a 200MHz

2

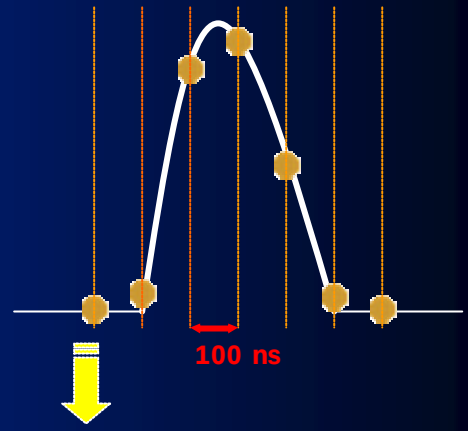
Control Unit supervises the working state of the 2 LIRA.

If a LIRA ends its writing phase and the other is still reading one have dead time.

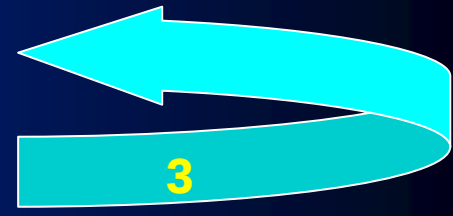
Optical Module Electronics (1)

Working principles

1. A 16 bit counter counts Master Clock cycles.
   - A FIFO stores data coming from the counter.
2. In the read phase LIRA transfer a suitable number of samples (anode o dynode) to a 10 bit 10 MHz commercial ADC.
3. The sampled Master Clock, Hi or Low, is stored in a suitable logic to give fine informations relative to the arrival time of the signal respect to the Master Clock.
4. Once a LIRA has been read and data have been converted by the ADC, the last is put by Control Unit in the Power Down state.
5. In few Clock cycles, anyway, ADC is ready to convert again.
6. Data flow going to the Concentrator is administrated by Control Unit through Data Packing and Transfer Unit.
7. Data are realligned, labelled, compressed and packed.

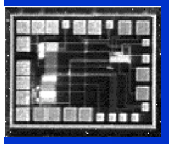


Encoding ADC 10 bit 10 MHz



The first LIRA completed the read phase and waits a new trigger. The other one now is ready to be read.

ADeLine2 not testable.

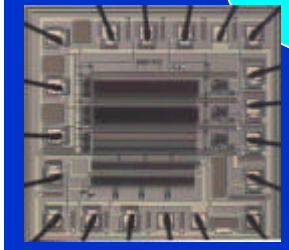


ADeLine1
0.7x1.1 mm²

1997

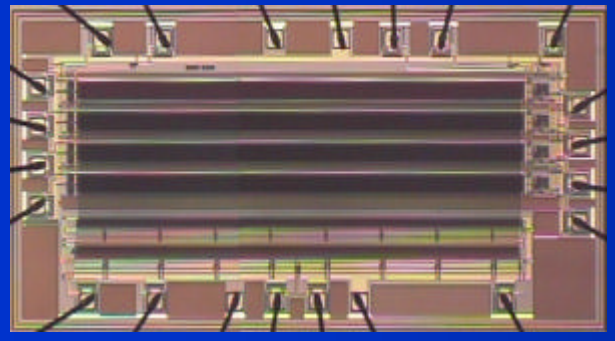
ADeLine3
1.4x1.3 mm²

I/1998



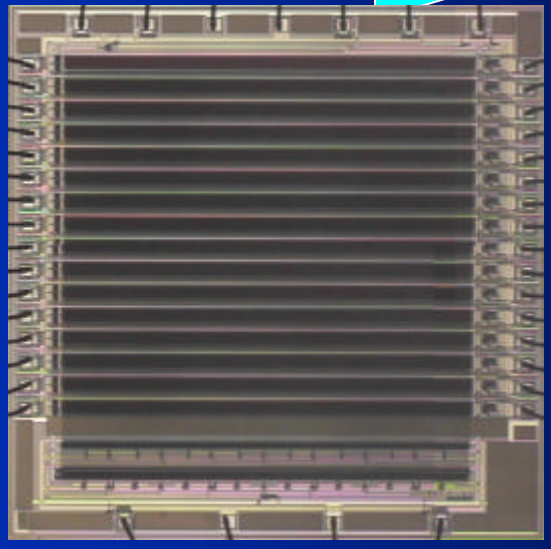
II/1998

ADeLine4
3.5x1.6 mm²



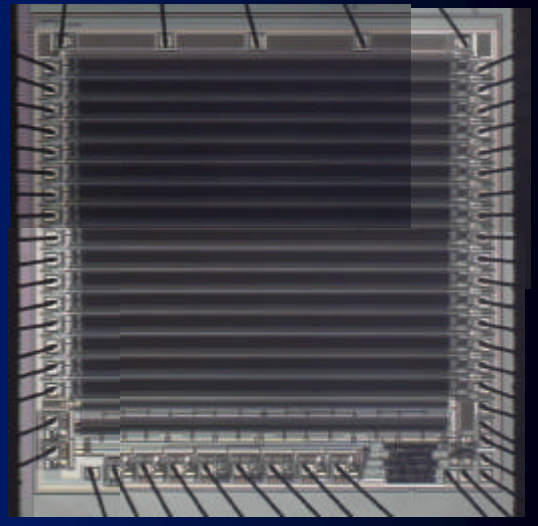
I/1999

ADeLine5
4.1x3.6 mm²

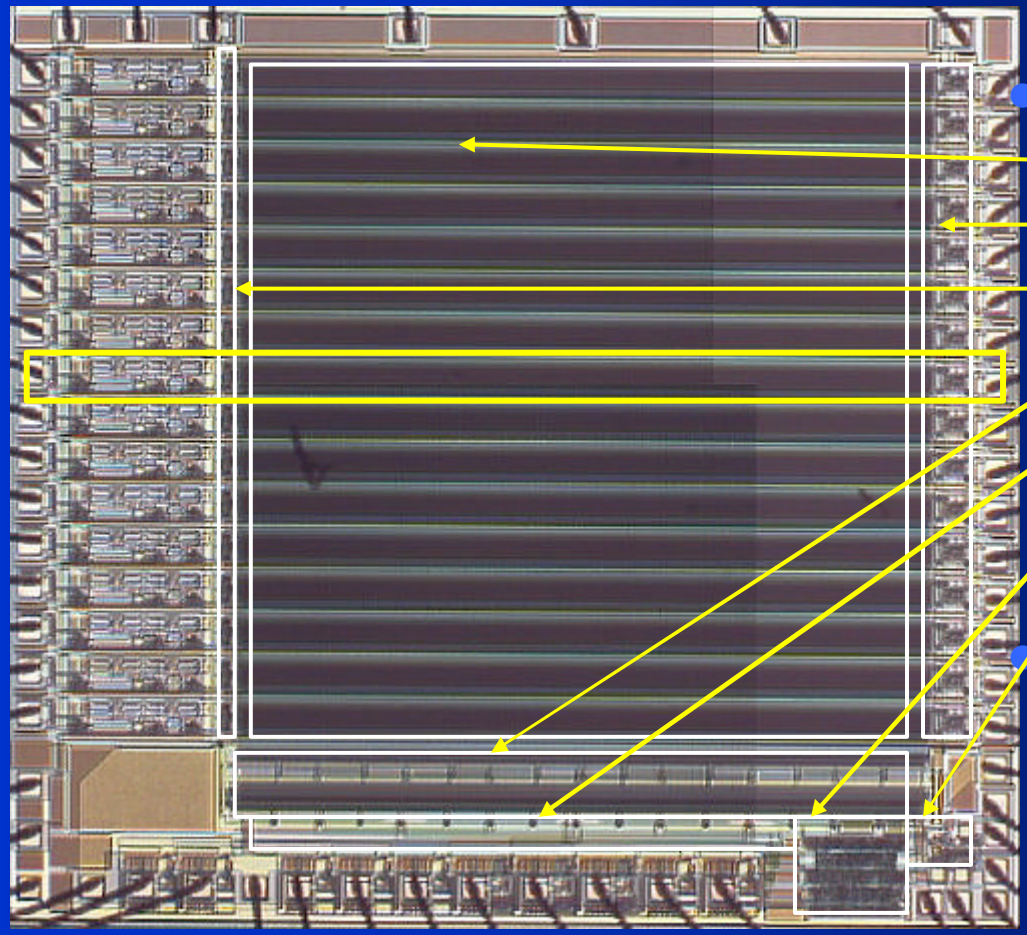


II/1999

ADeLine6
4x3.5 mm²



ALICE chip

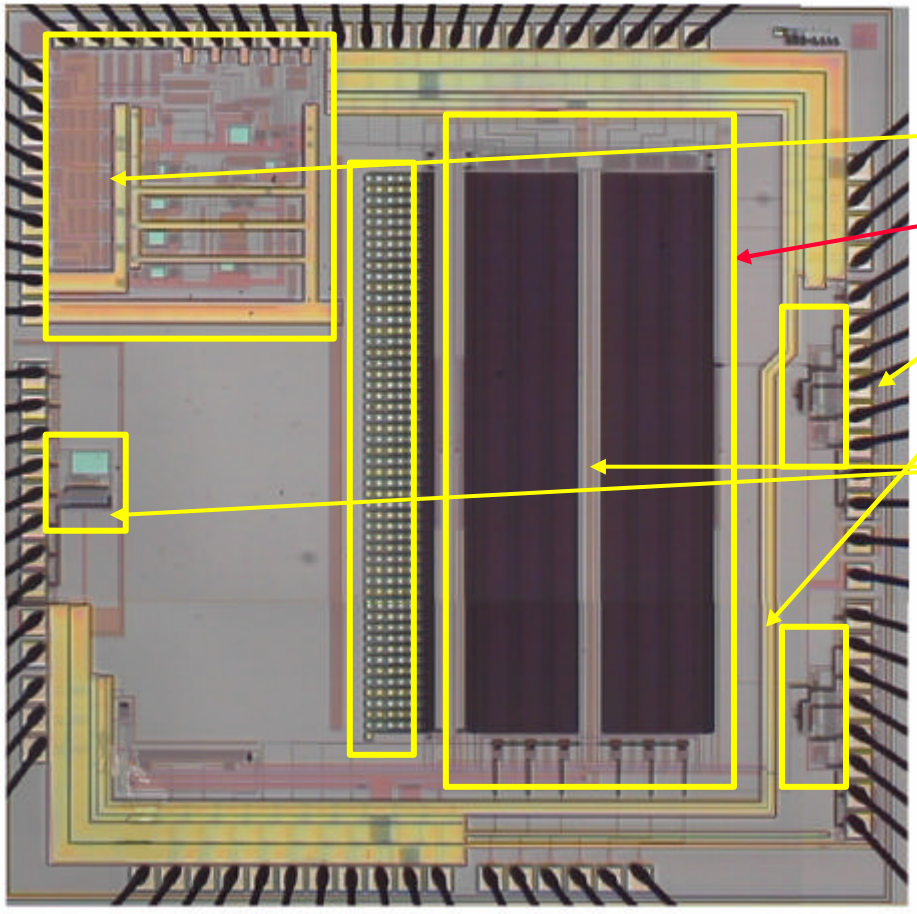


- ADeLIAS microphotography
  - switched capacitors array
  - readout buffers
  - input switches
  - addressing unit
  - clock distribution net
  - digital control unit
  - analogue control unit
- AMS CYE technology
  - 0.8 um standard CMOS
  - double poly double metal

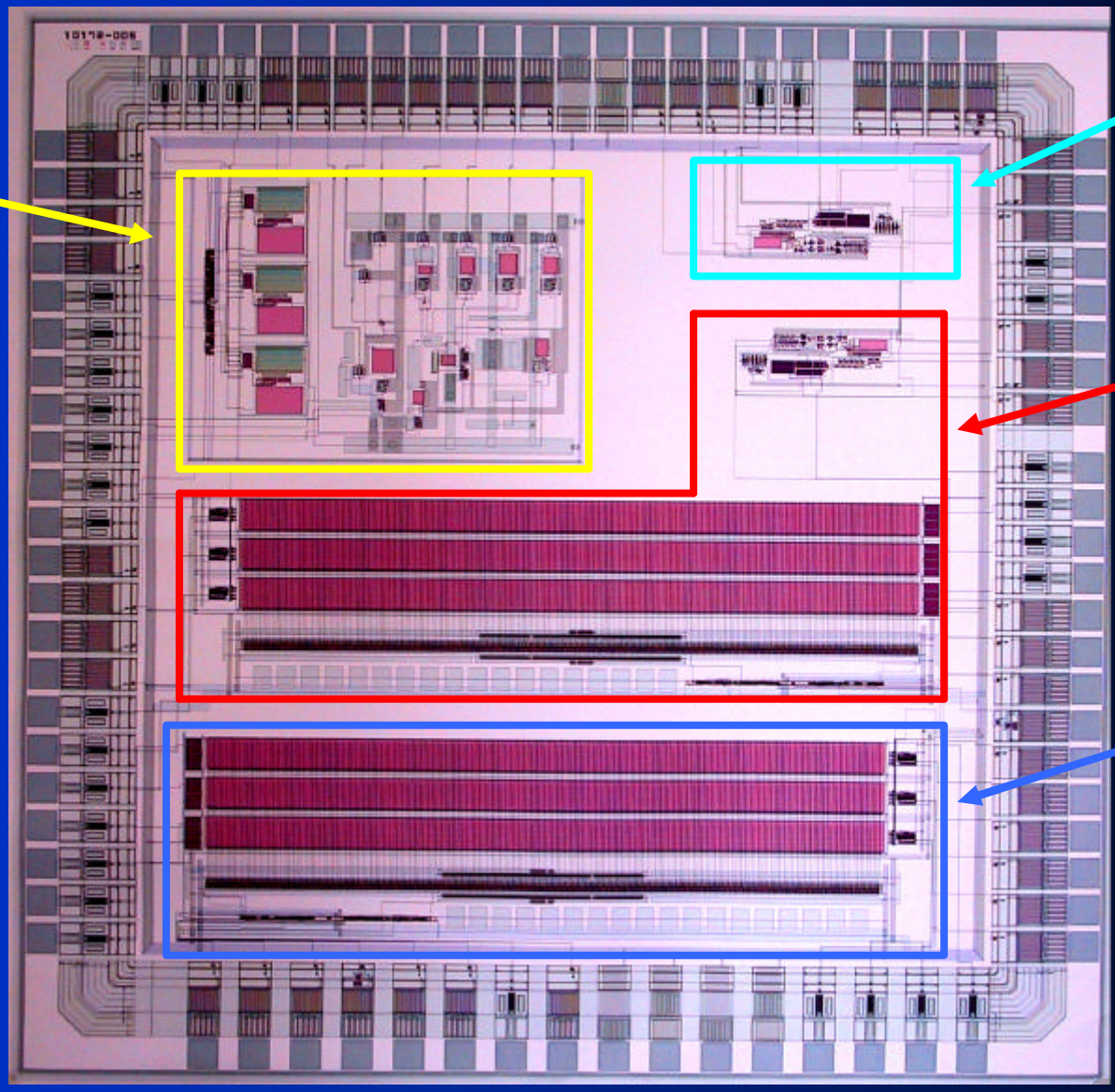
Design Specifications

Specifications:	0.8 μm CMOS	0.35 μm CMOS
– Write/Read frequencies	40/1 MHz	200/10 MHz
– Cells x channels	256 x 16	256 x 3
– Power/channel	< 4 mW	minimum
– Linear range	1 V	1 V
– Resolution	8 bit	8 bit
– Pedestal variation	< 2 mV	< 2 mV
– Capacitive load	15 pF	7 pF

AMS CSD chip



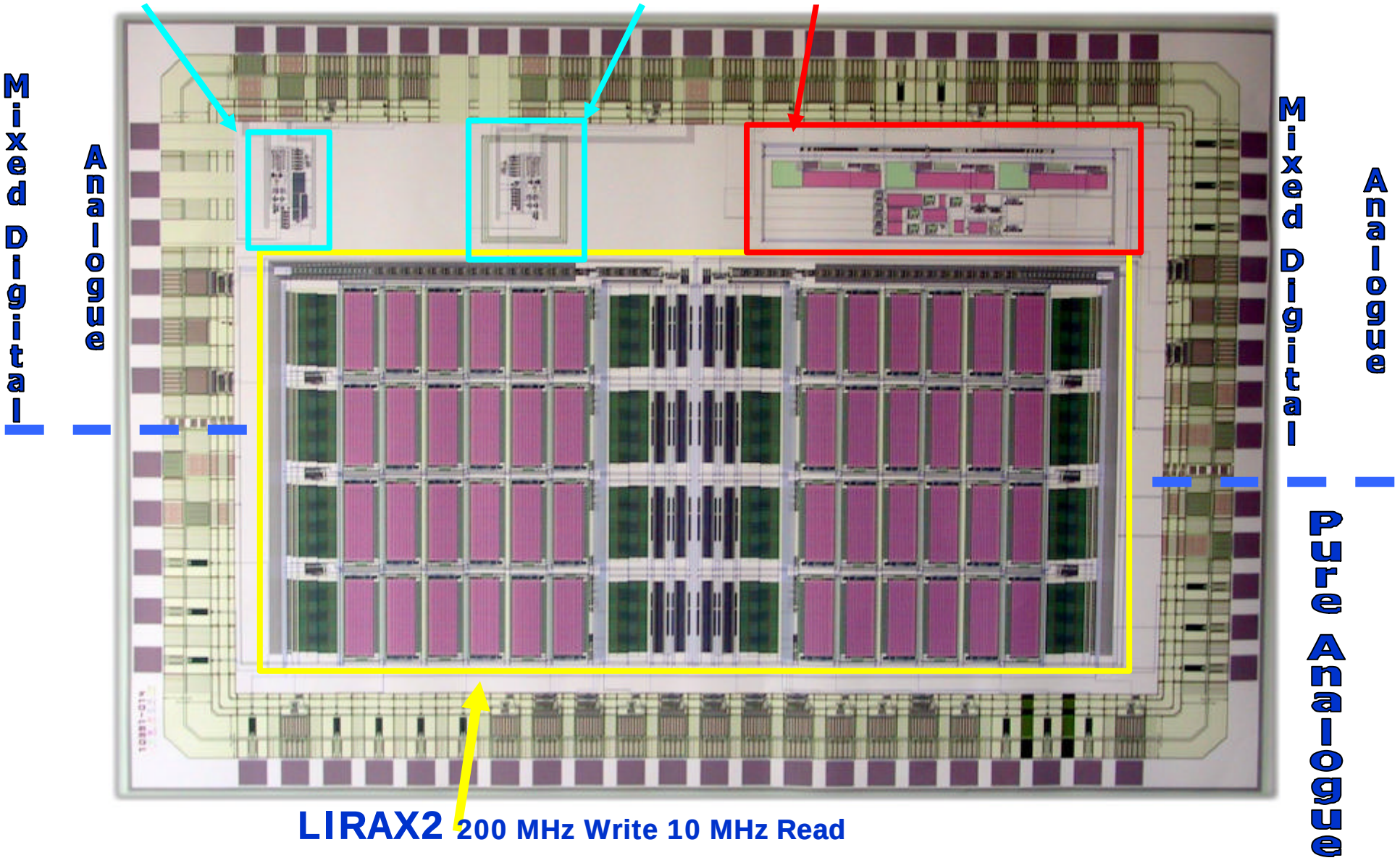
- LIRA01 microphotography
  - 200 MHz PLL
  - analogue memories
  - DAC
  - Trigger and Classification Unit
  - Test structures
- AMS CSD technology
  - 0.35 um standard CMOS
  - double poly triple metal



Packed

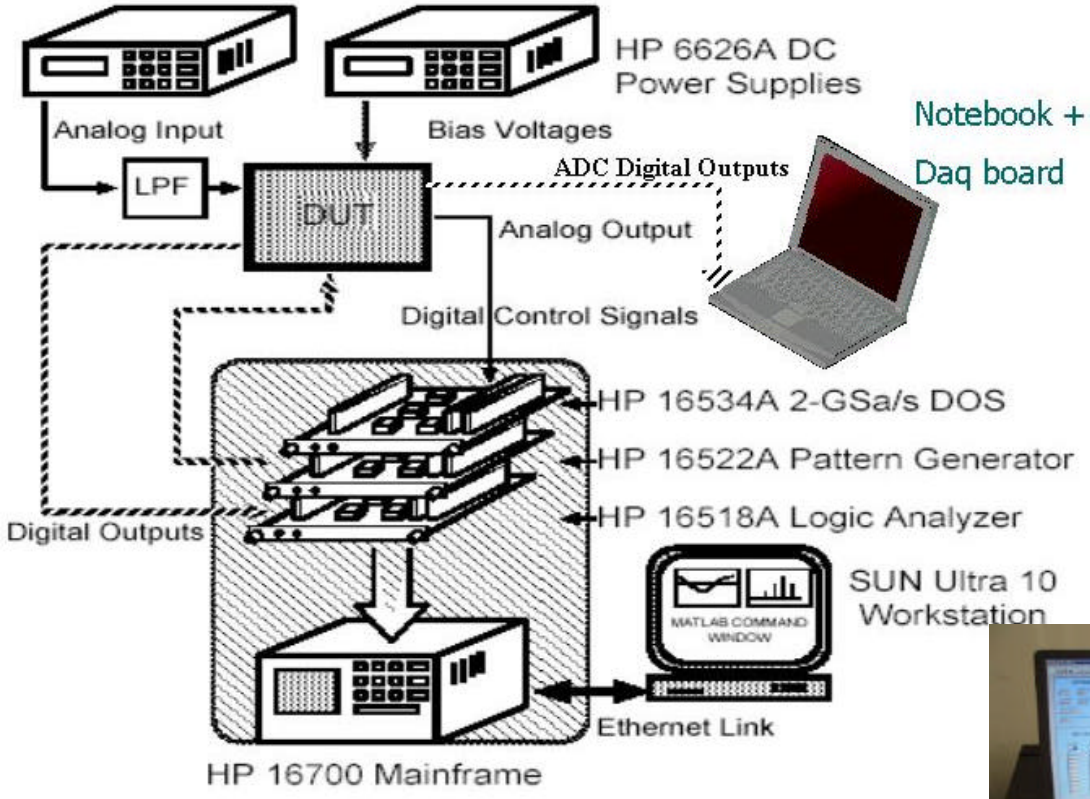
JLCC84 – 84 pin

LIRA02 Chip AMS 0.35 μm Area=10 mm²


PLL Stand Alone 200 MHz
Slave Clock Generator
LIRA's PLL
Shielded
T&SPC
Substrate decoupling
Mixed Digital
Analogue
Mixed Digital
Analogue
Pure Analogue
LIRAX2 200 MHz Write 10 MHz Read

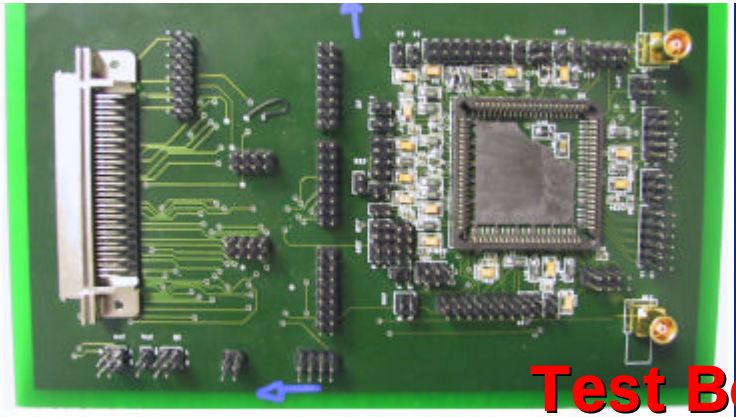
LIRA03 CHIP

Test Setup

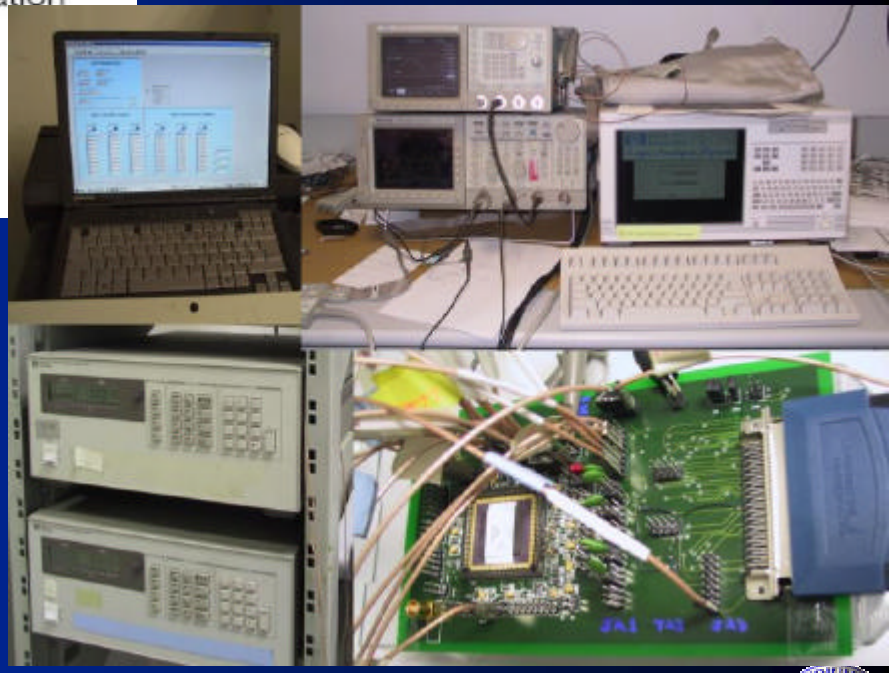


Software DAQ

Dedicato (LabView)



Test Board



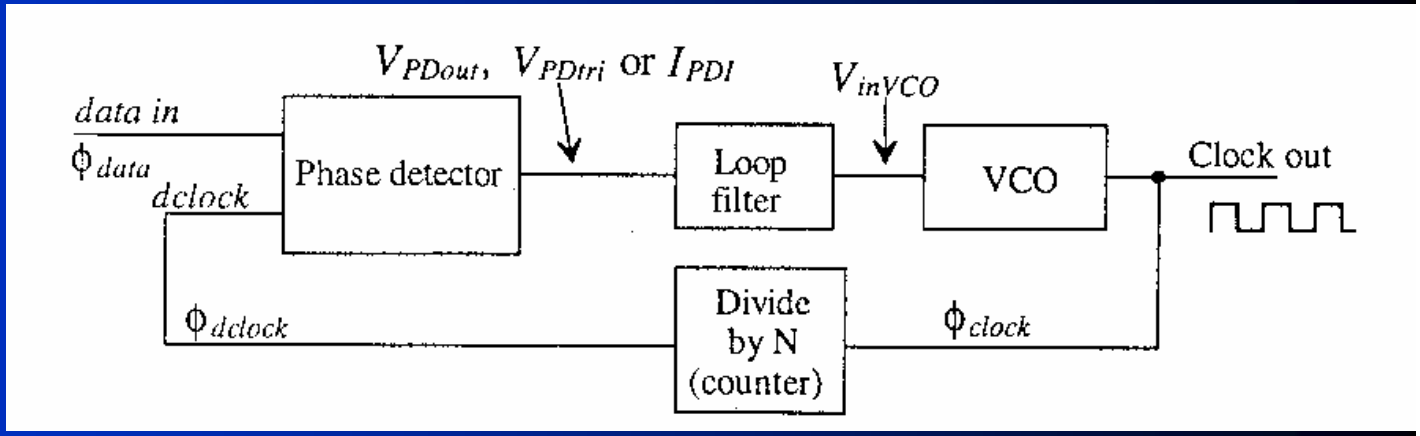
TEST RESULTS
CHIP LIRA02

PLL Stand Alone 1

Data in = Master Clock a 20 MHz

Clock out = Slave Clock a 200 MHz

N=10



I/O frequency ratio adjustable → $V_{control}$

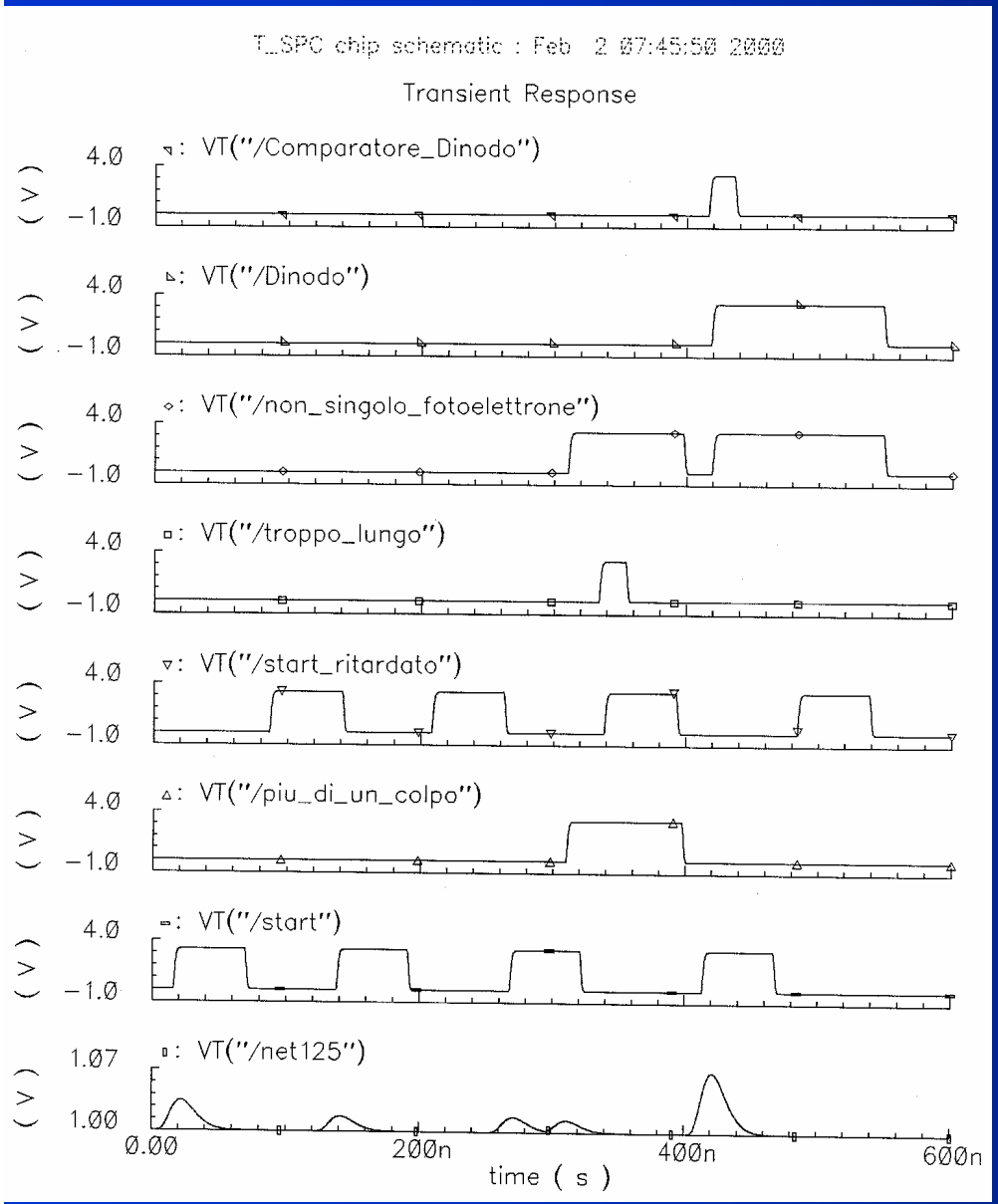
- **All the blocks work properly except VCO**

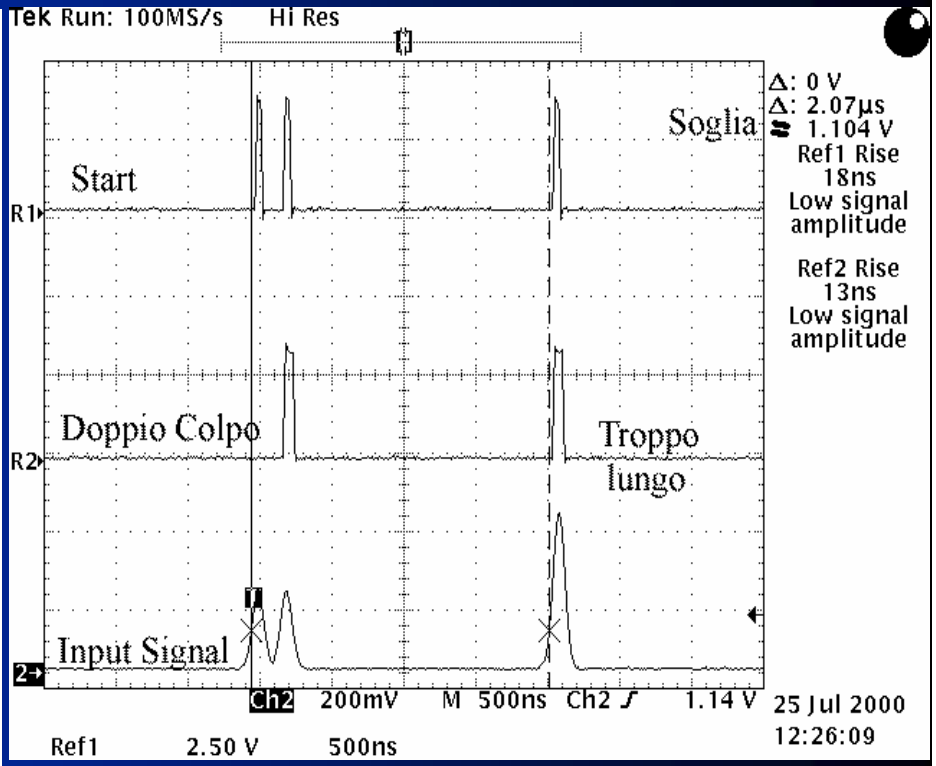
Clock out frequency < 200 MHz

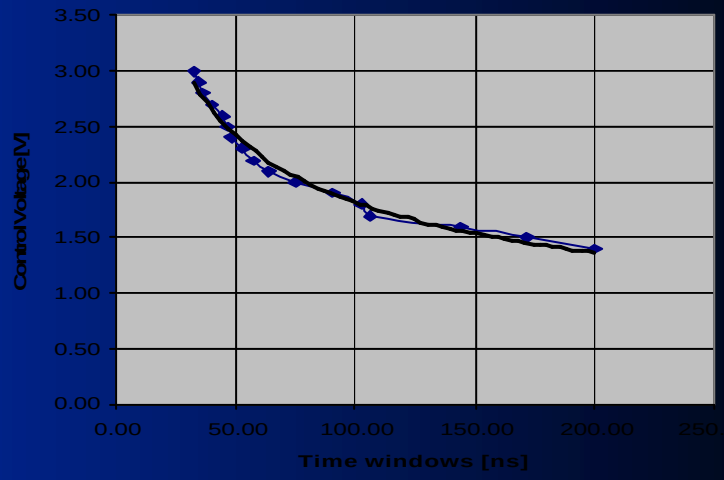
SC » 144 MHz ($V_{control}$) on phase with MC ($N_{divider}$=8)

Parasitics Underestimation in the internale stages of VCO

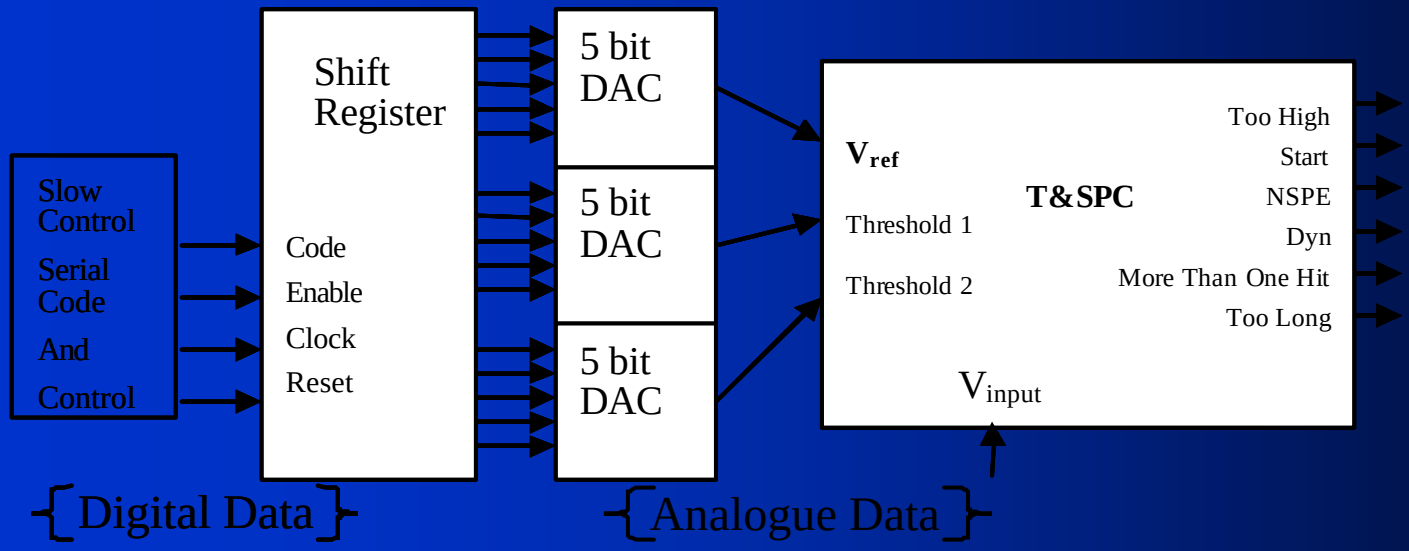
Trigger & Single Photon Classifier

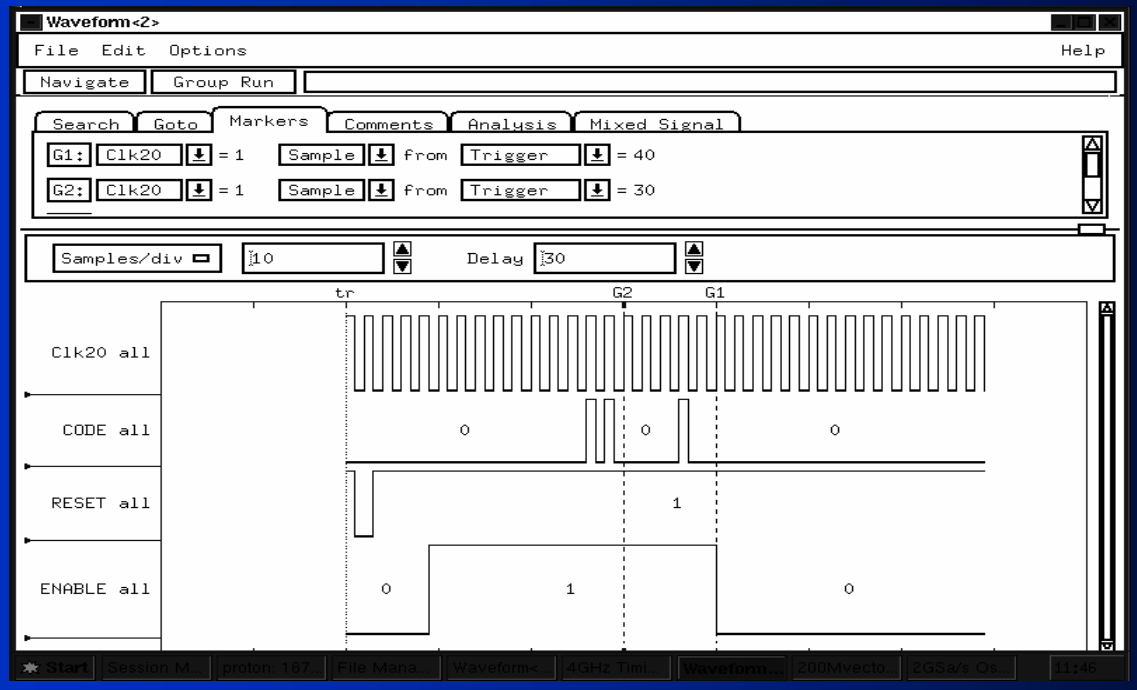




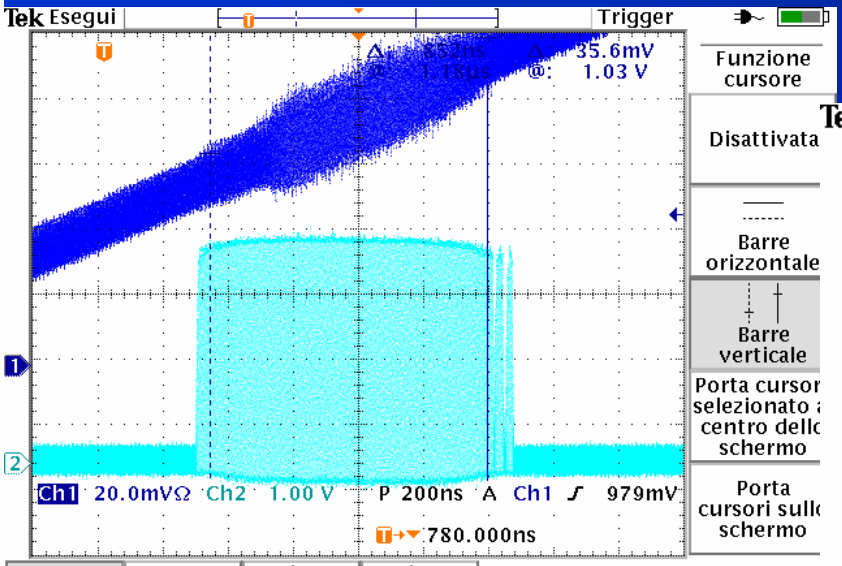


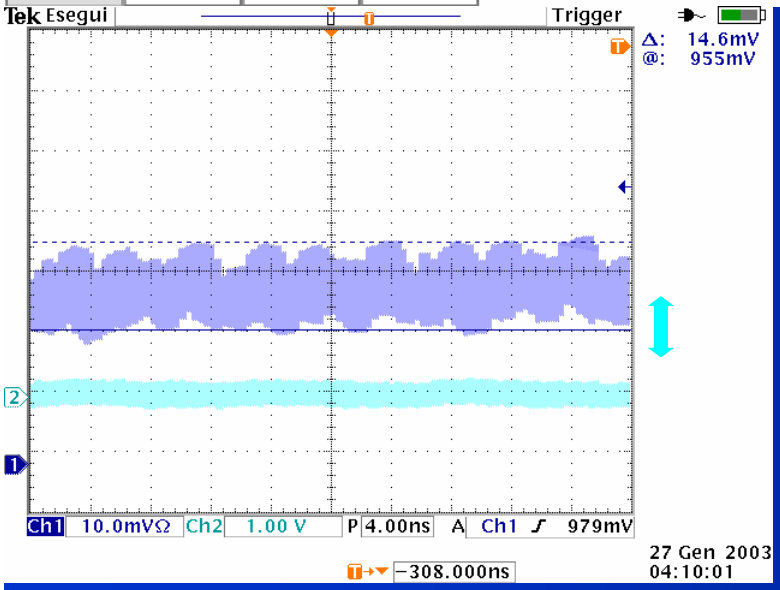
Slow Control Interface

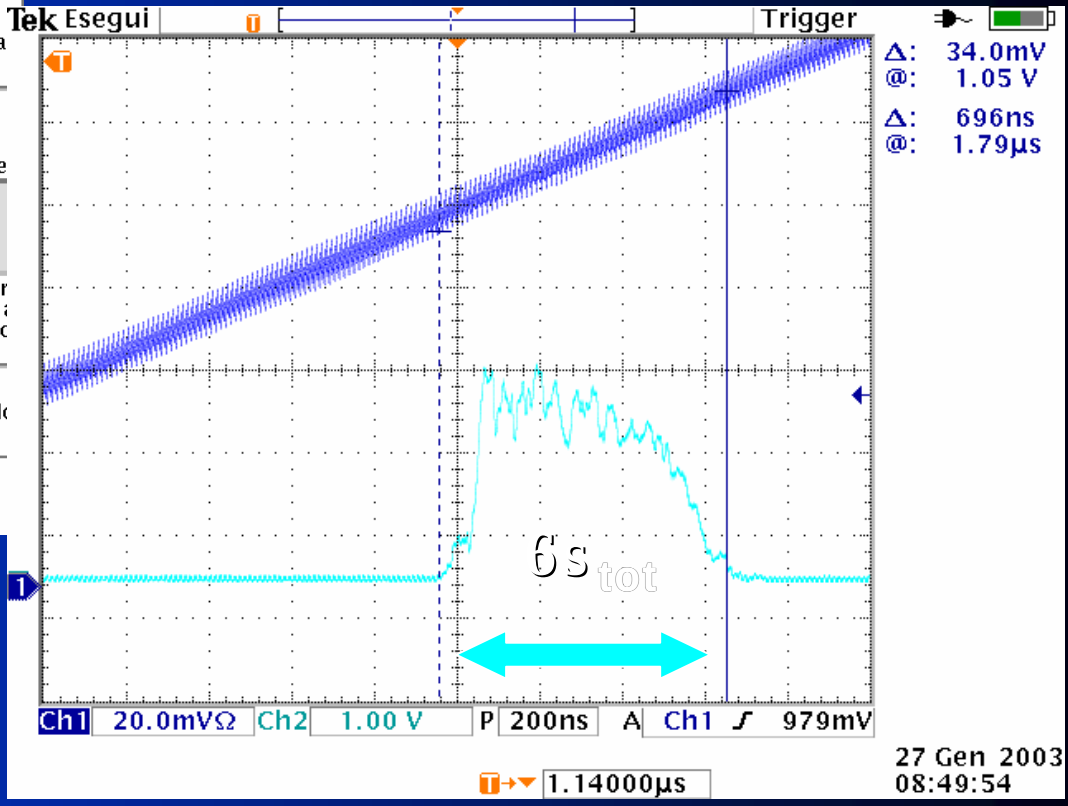




T&SPC Comparator Resolution





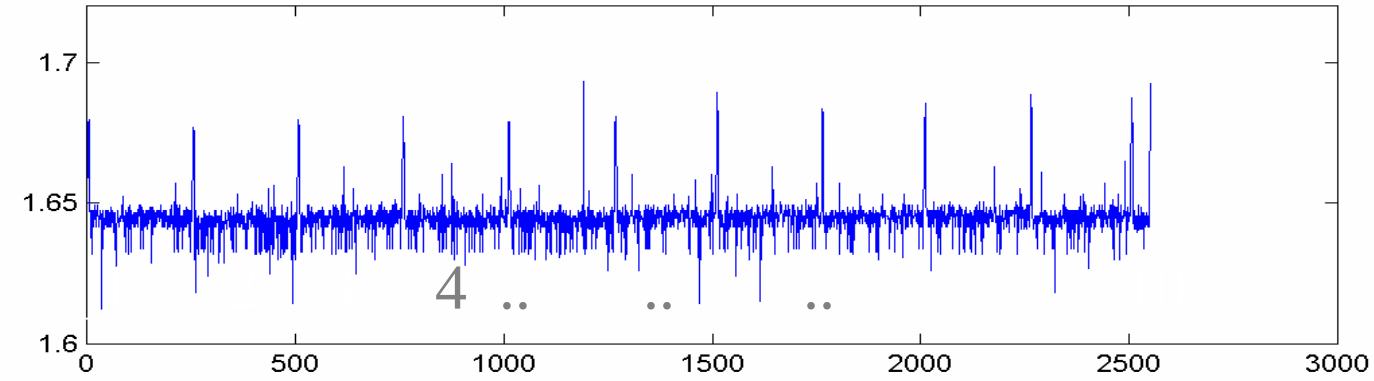


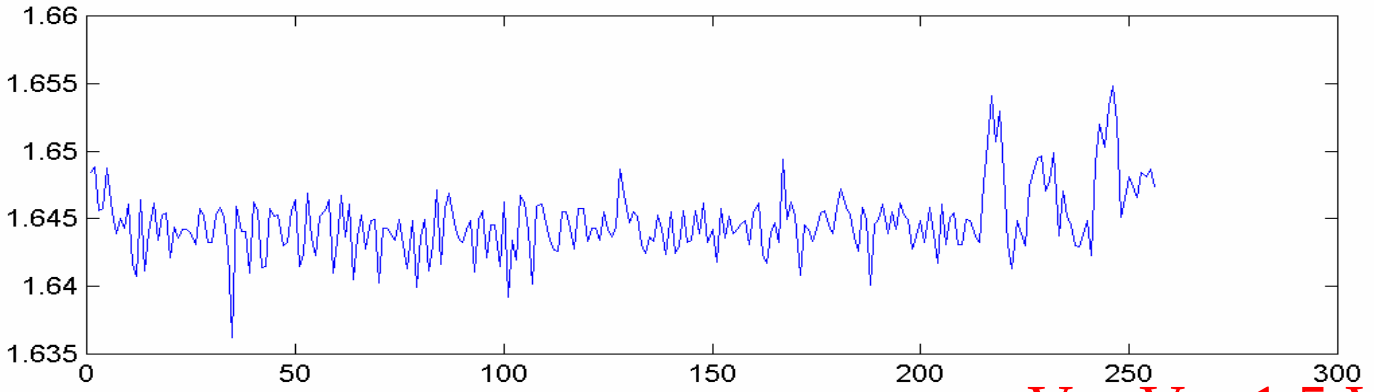
RMS = σ_{Noise}

σ_{comp} @ 5 mV

LIRA TEST RESULTS

Dat File (256×10 samples) acquired in the NI DIO32 board by the ADC 3 corrisponding to LIRA alone channel 3. 100 MHz sampling rate – 5 MHz readout rate @ V_{IN} = 2.1 V.

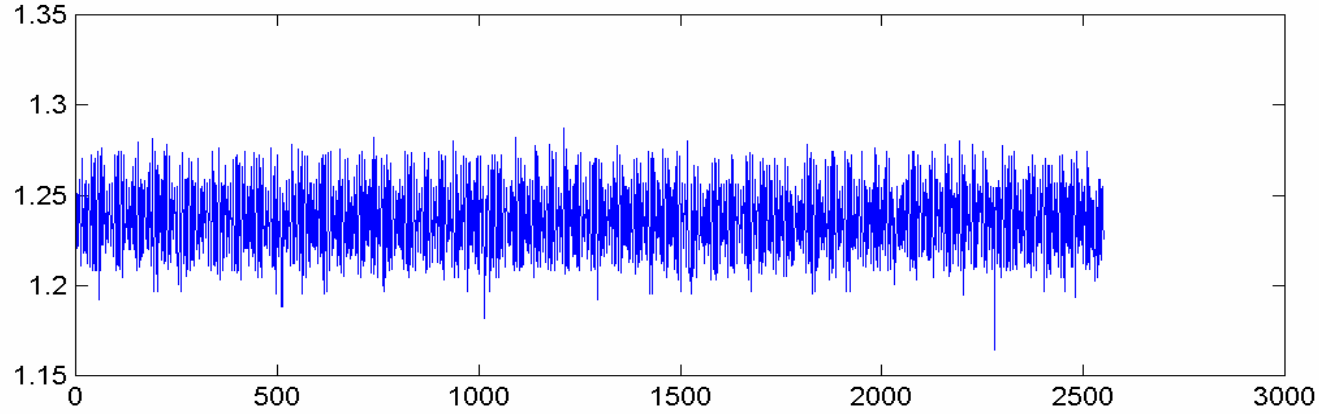


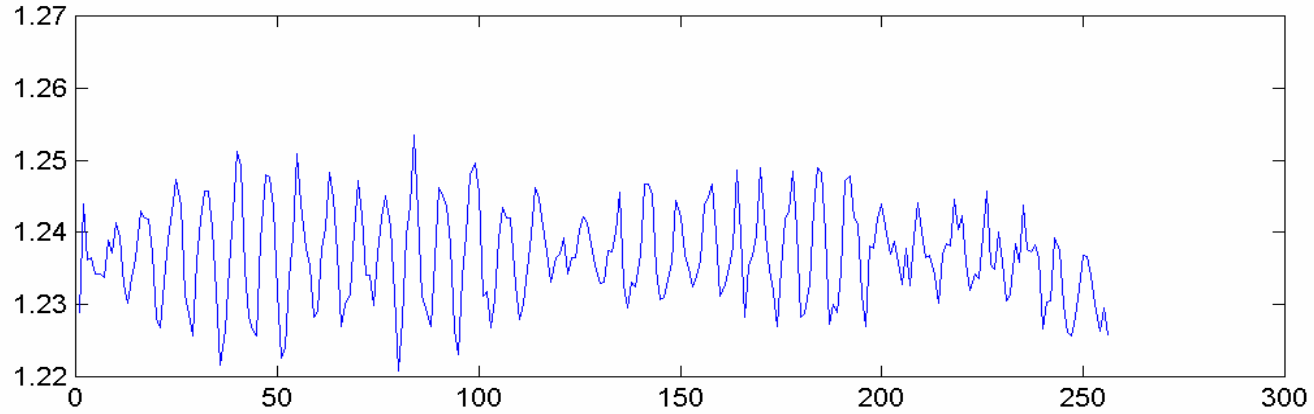


V_A=V_B=1.5 V

Corrisponding Dat file (256 samples- 10 times averaged).

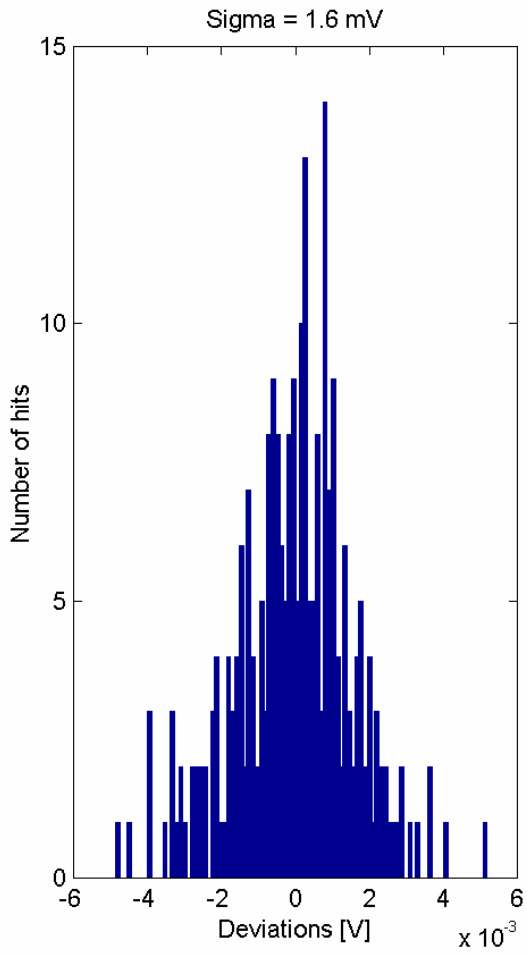
Dat File (256×10 samples) acquired in the NI DIO32 board by the ADC 3 corrisponding to LIRA alone channel 3. 100 MHz sampling rate – 10 MHz readout rate @ V_{IN} = 1.5 V.

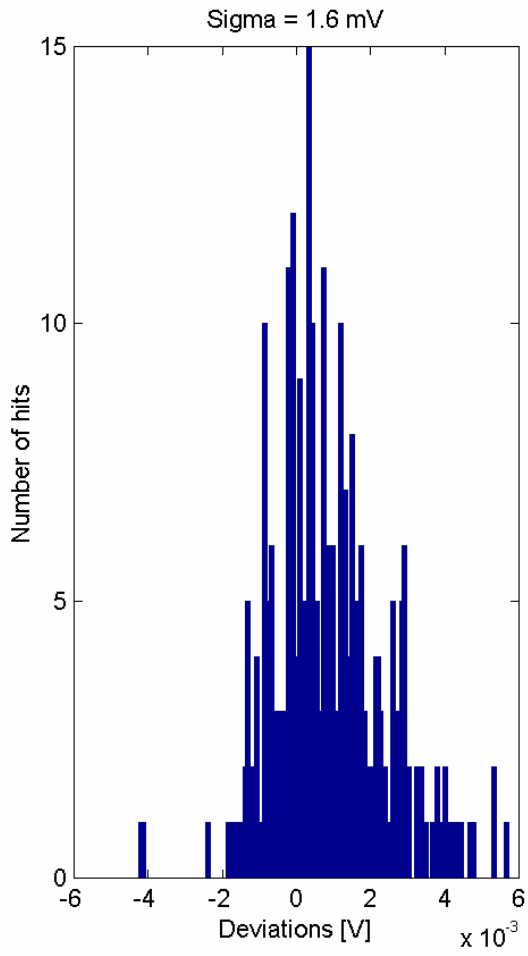




Corrisponding Dat file (256 samples- 10 times averaged).

Pedestal-subtracted value histogram for channel 3 @ 100 MHz sampling rate – 5 MHz readout rate and V_{IN}=1.2 V (left) V_{IN}=2 V (right)





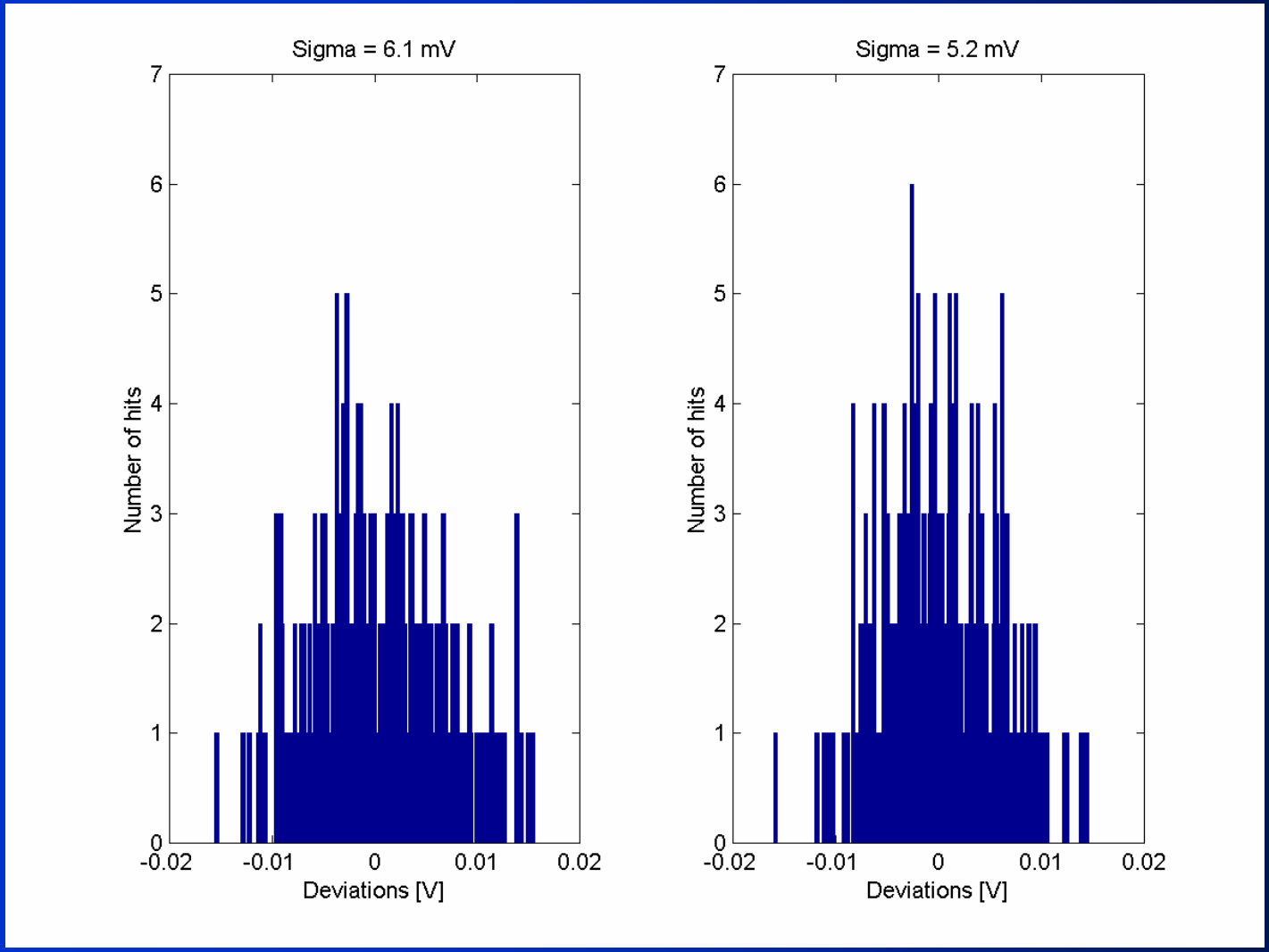
$$\overline{x_j} = \frac{1}{\text{Number of Acquisition}} \sum_k x_{j_k}$$

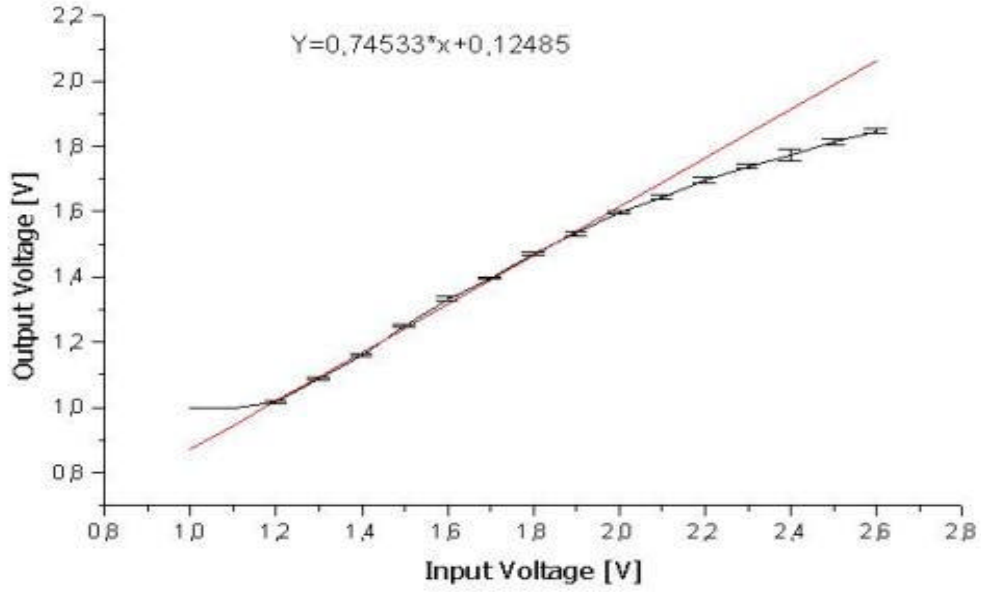
$$V_{\text{ped}_j} = \overline{x_j} - V_{\text{in}}$$

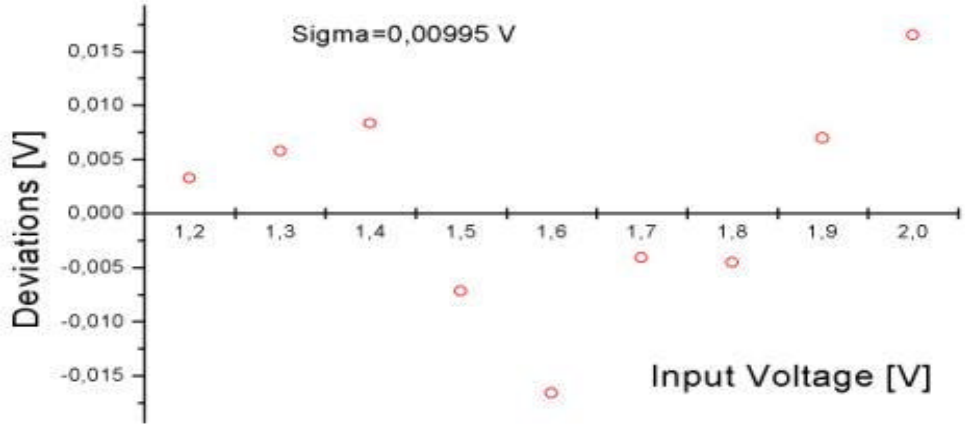
$$\Delta V_{\text{ped}_{j_k}} = (x_{j_k} - V_{\text{in}}) - (\overline{x_j} - V_{\text{in}}) = x_{j_k} - \overline{x_j}$$

V_A=V_B=1.5 V

Pedestal-subtracted value histogram for channel 3 @ 100 MHz sampling rate – 10 MHz readout rate and V_{IN}=1.5 V (left) V_{IN}=2 V (right)

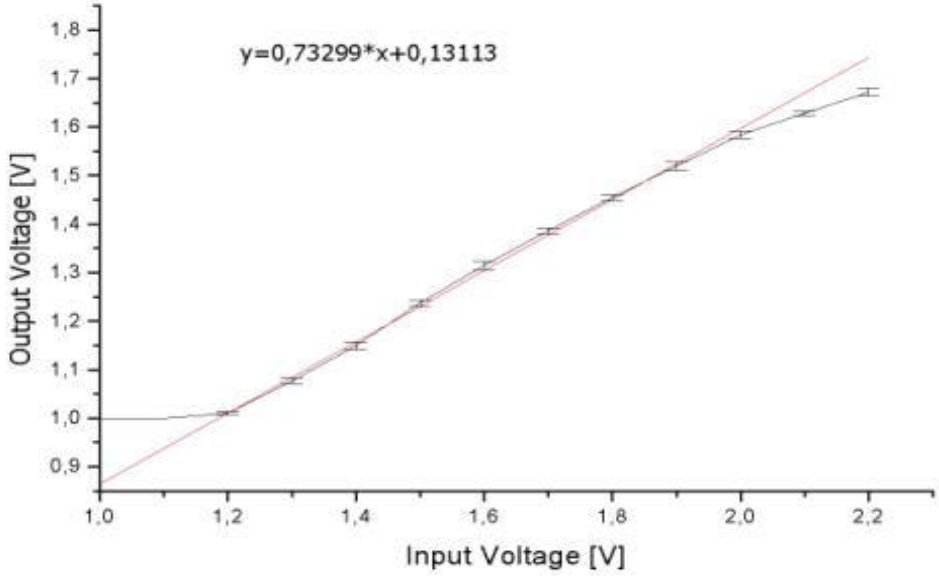


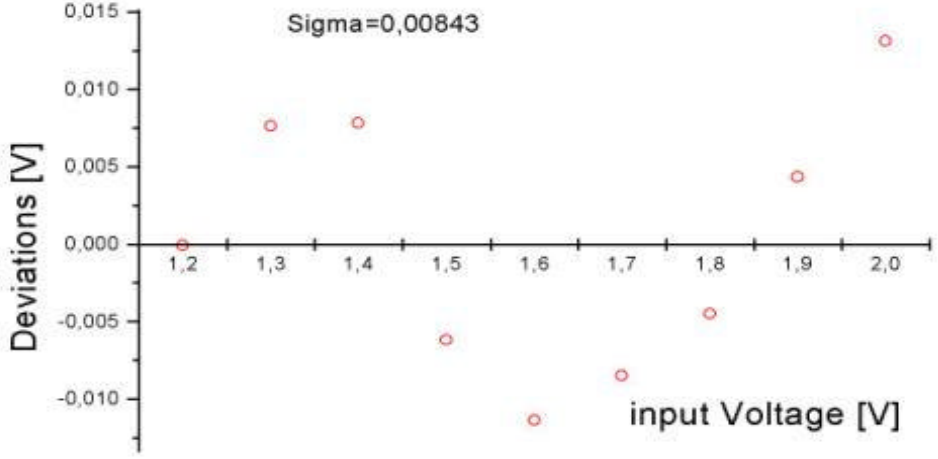




(**Top**) Channel 3 average output as a functon of the input voltage @ 100 MHz sampling rate, 5 MHz read-out rate.

(Bottom) Deviations from linear fit in the selected linear range 0.8 V @ 100 MHz sampling rate, 5 MHz read-out rate.





(**Top**) Channel 3 average output as a functon of the input voltage @ 100 MHz sampling rate, 10 MHz read-out rate.

(Bottom) Deviations from linear fit in the selected linear range 0.8 V @ 100 MHz sampling rate, 10 MHz read-out rate.

Total power dissipation

Maximum power dissipation for the whole chip has been measured using the instantaneous current value on the the two power supply HP 6626A.

I_{Amax} = 8.78 mA

$V_{DDD}=V_{DDA}=V_{DD}$= 3.3 V → PD=225 mW

I_{Dmax} = 59.6 mA

Relative to 2 PLL, 2 AM LIRA (200 MHz write frequency (w.f.) and 10 MHz readout frequency (r.f.)) and T&SPC working state.

Readout

LIRA02 chip satisfies the specification of 10 MHz readout frequency. The results for 10 MHz and 5 MHz are quite similar. Some optimization is needed to have the best performances.

Linearity

AM Linearity range, 0.8 V @ 100 MHz w.f. and 5 MHz r.f. influenced by non unitay gain -> 0,75.

•Readout OTA gain too low.

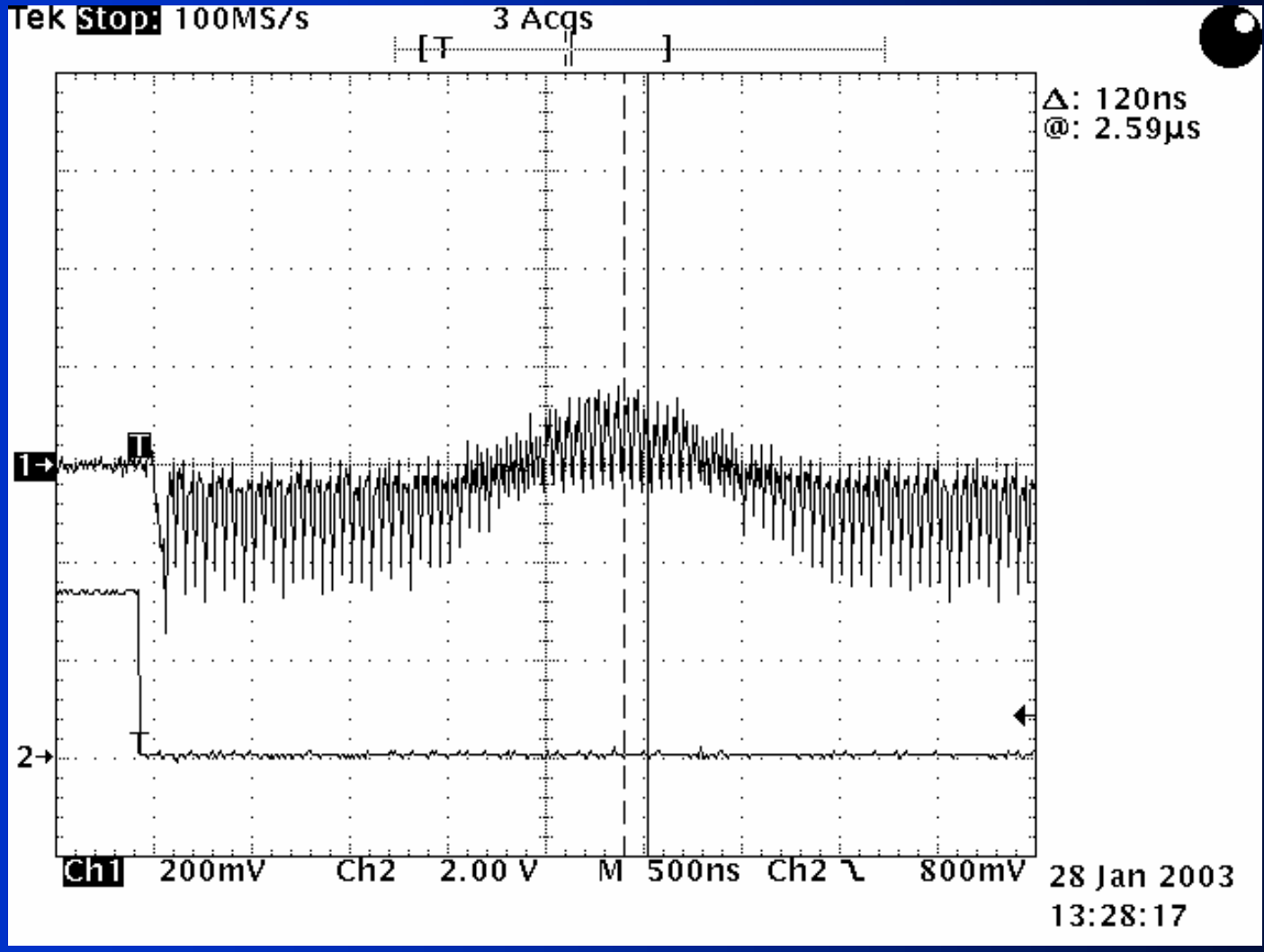
Dynamic Range

Sampling Rate [MHz]	Readout Rate [MHz]	Pedestal resolution [mV rms]	DC gain	Linearity resolution [mV rms]	Linear range [V]	Total resolution [bit]
100	10	5.5	0.733	2.81	0.8	8
100	5	1.6	0.745	3.32	0.8	8

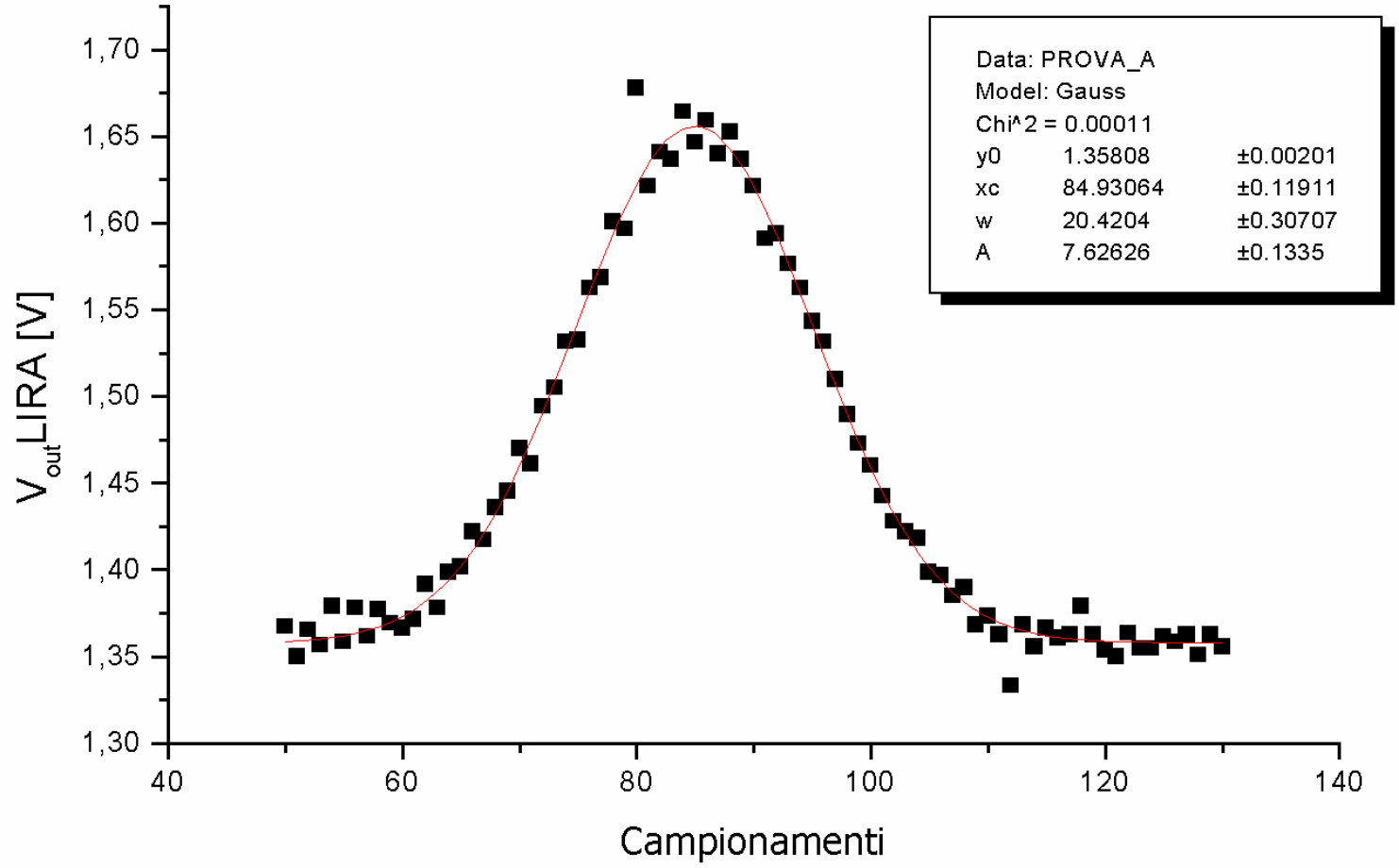
LIRA AC performances test

- AC Test of LIRA possible only after control signal modification
- Memory addressing with simulation signals not correct
- Possible cause → malfunctioning of the memory control logic used to synchronyze the control signals to Master clock
- AM write phasis perfomed using, missing the PLL, an external generator.

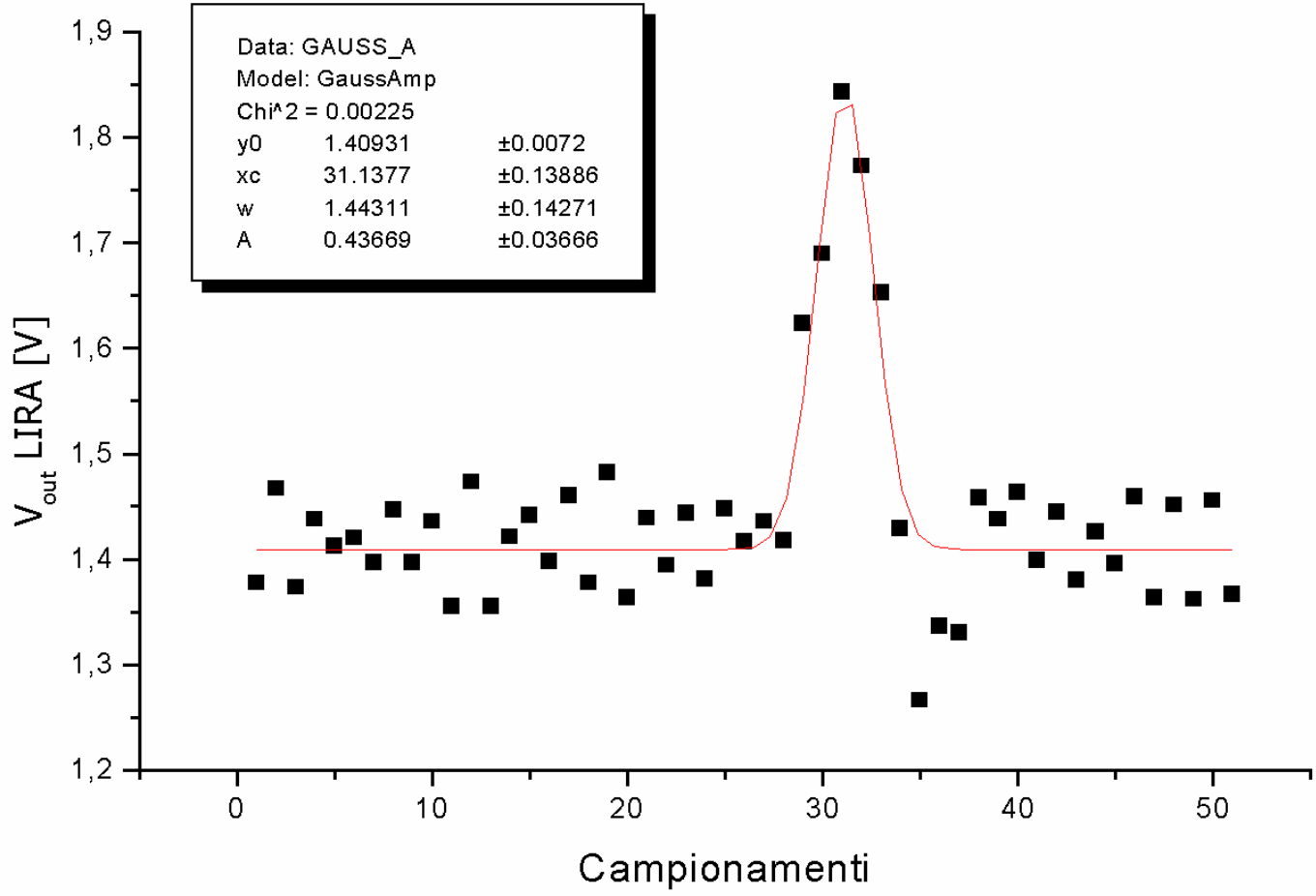
Gaussian signal sampling
LIRA02 100MHz W 10MHz R



Gaussian signal Reconstruction
LIRA02 100MHz W 10MHz R



Gaussian signal Reconstruction



CONSIDERATIONS ON TEST RESULTS - LIRA02

- PLL
  - VCO Layout → parasitics reduction
  - Total layout Optimization
- LIRA
  - Redesign logic
  - Readout Buffer
    - Redesign
    - New architecture with readout and write bus separated
- TSPC + Interfaccia Slow Control
  - Optimize layout

CONCLUSIONS

- **Starting from a KM³ underwater Cherenkov ν detector sperimental demands :**

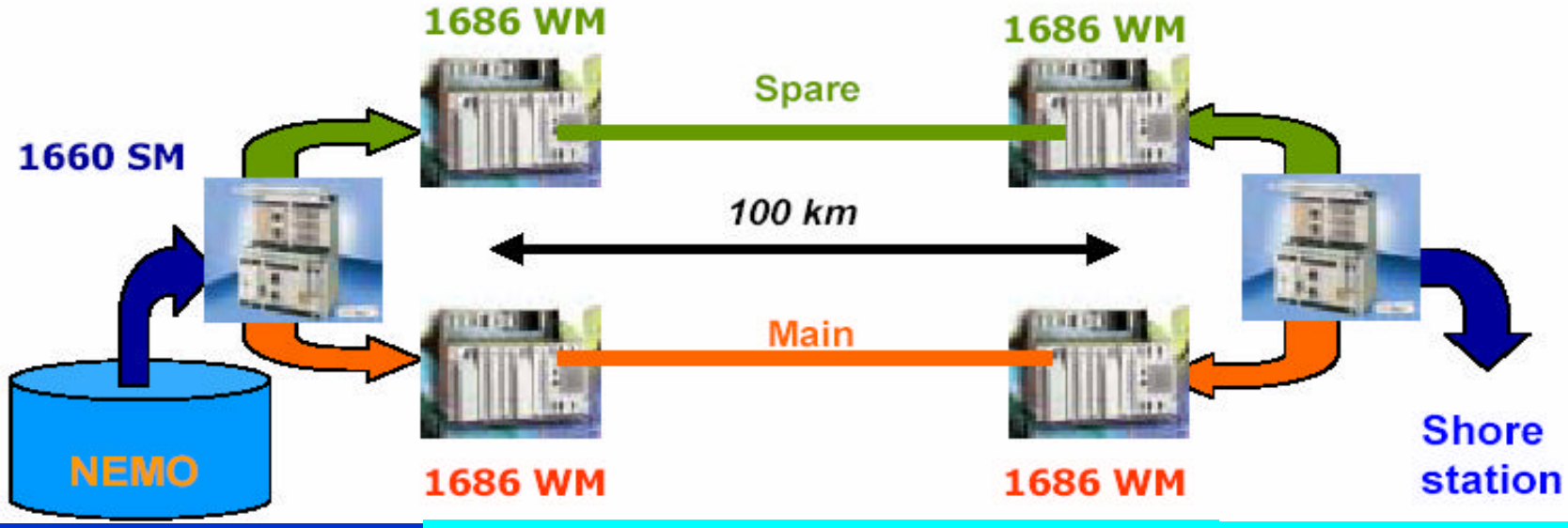
  ASIC VLSI OM front-end design

- **Construction of a chip front-end prototype**
- **Test and analysis of the results**

  Very encouraging results

- **Design of a new version**

Data flux in the detector



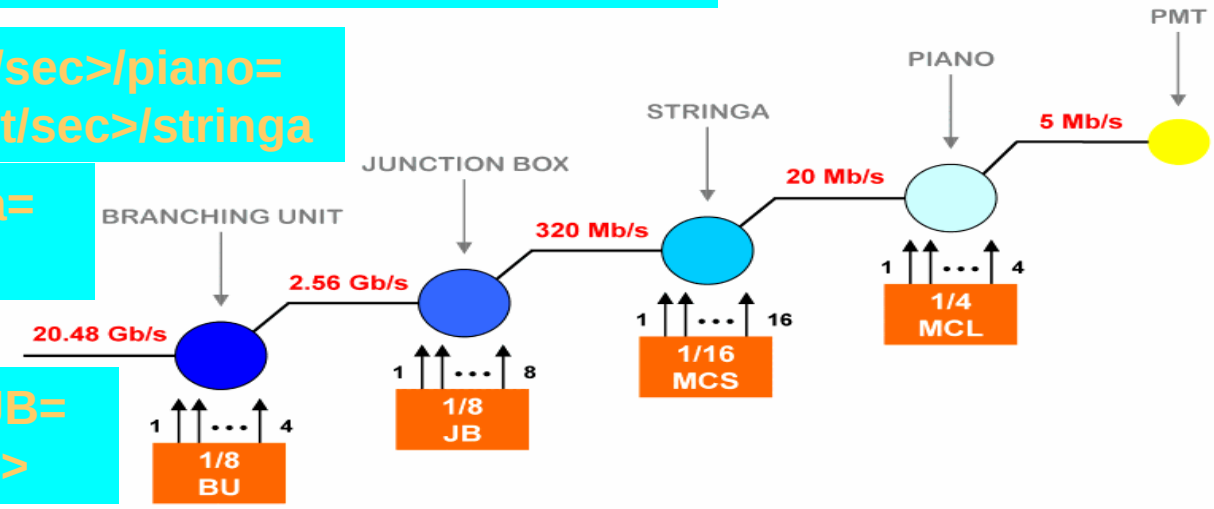
<50 Keventi/OM x 100bit/eventi>
= <5Mbit/sec>

<50 Keventi/OM>

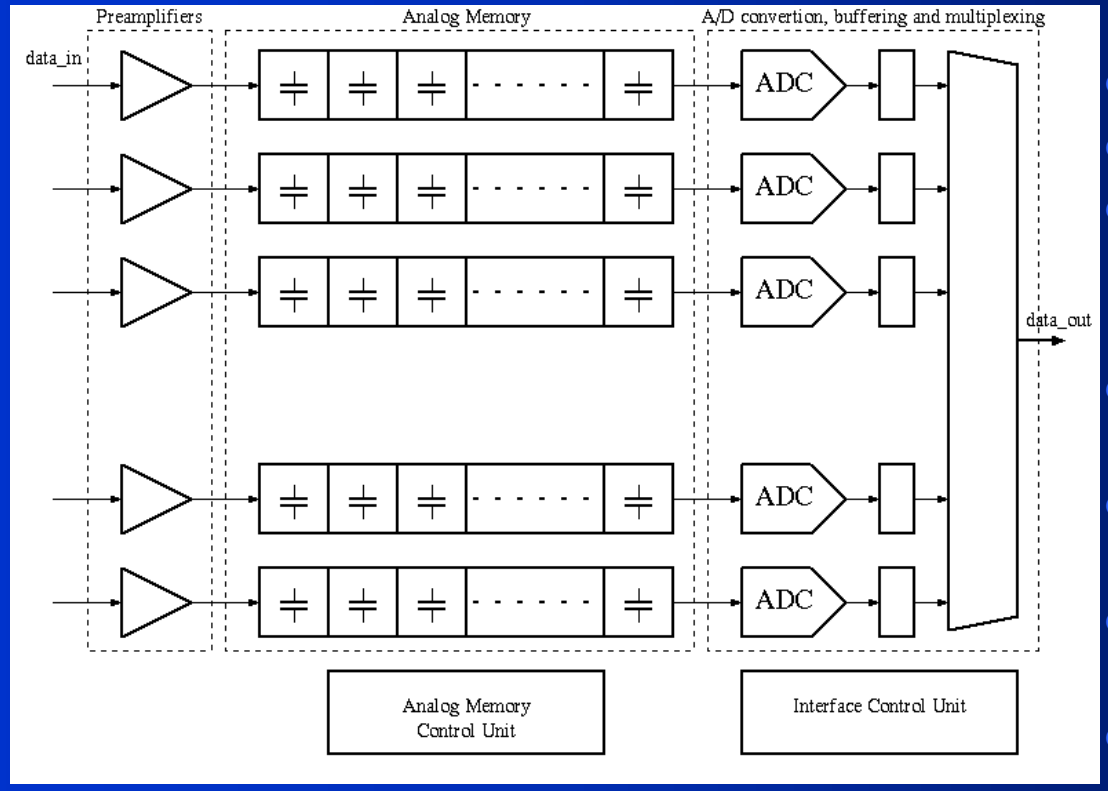
<5Mbit/sec>/piano=
<320Mbit/sec>/stringa

<320Mbit/sec>/stringa=
<2.56Gbit/sec>/JB

<2.56Gbit/sec>/JB=
<20.48Gbit/sec>



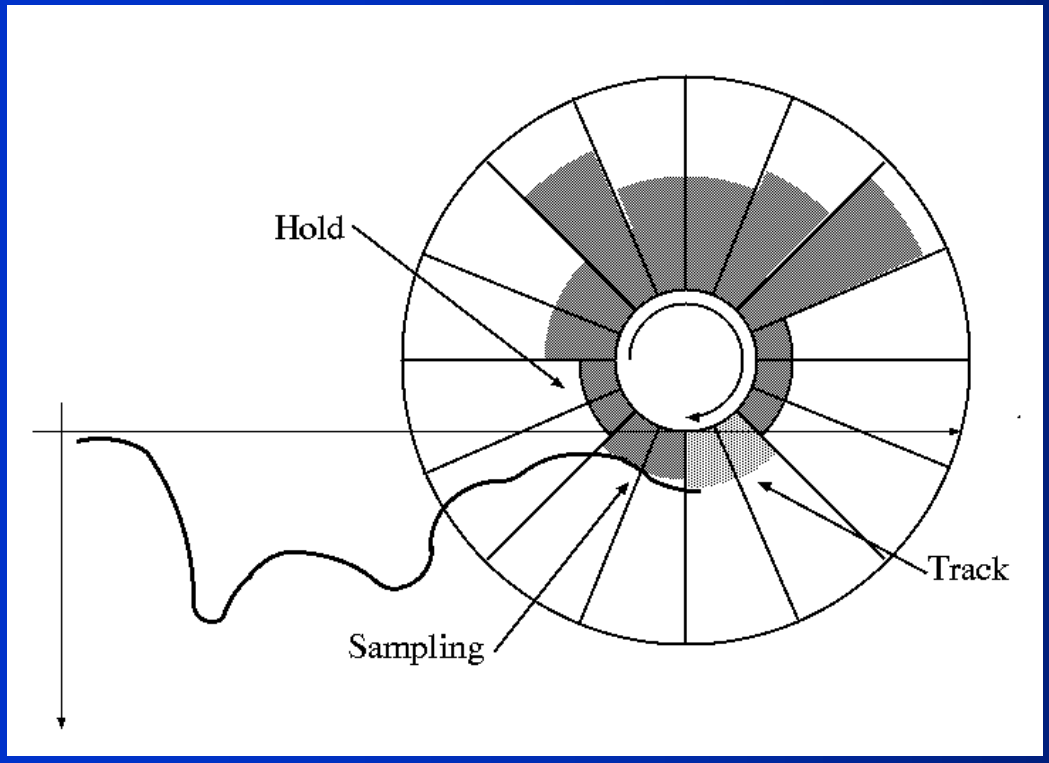
Role of Analogue Memories in Waveform Acquisition Systems



- Non repetitive input waveforms
- Only short part interesting
- Off-line data analysis
- Non continuous digitisation required

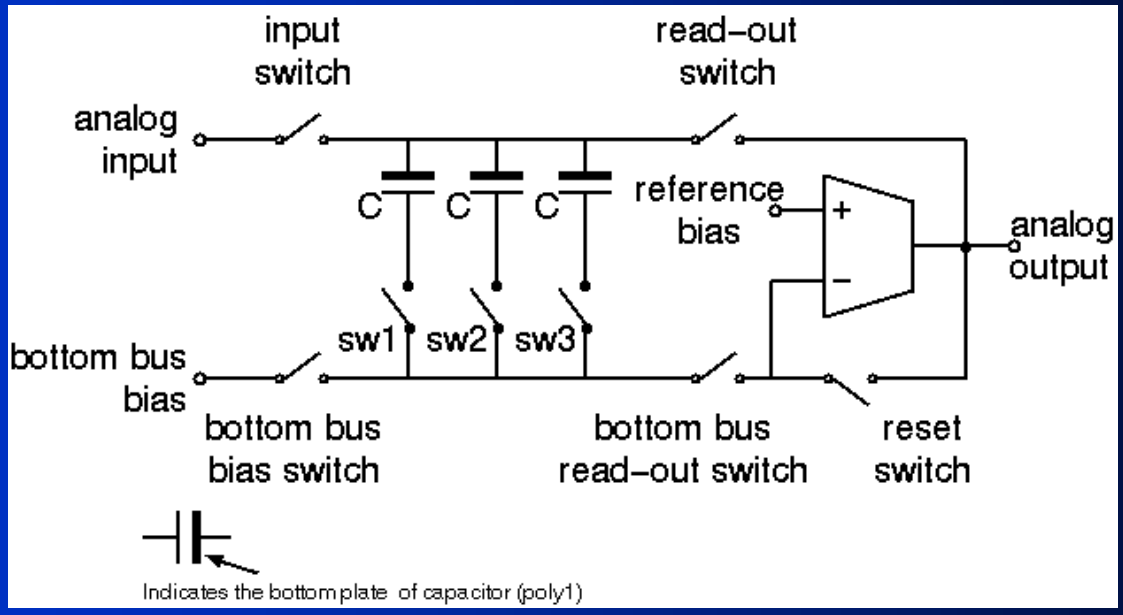
- Preamplifiers continuously write into memory
- Samples are stored into capacitive cells
- Memory is frozen at trigger occurrence
- Only memory contents is converted

Time Delaying Features



- Conversion starts only when data are validated
- Memory size lower limited by *validation time*
- Lower conversion rate than sampling rate
- Conversion rate lower limited by *dead time*

Schematic Diagram of Architecture



- cell pedestals doesn't depend on input signal
  - – could be determined and cancelled
- turn-off time of the sampling switches doesn't depend on input signal
  - – no timing error
- low cell-to-cell gain variation across a channel
- external (synchronous) controlled circular addressing scheme
  - – better sampling accuracy of high BW signals