

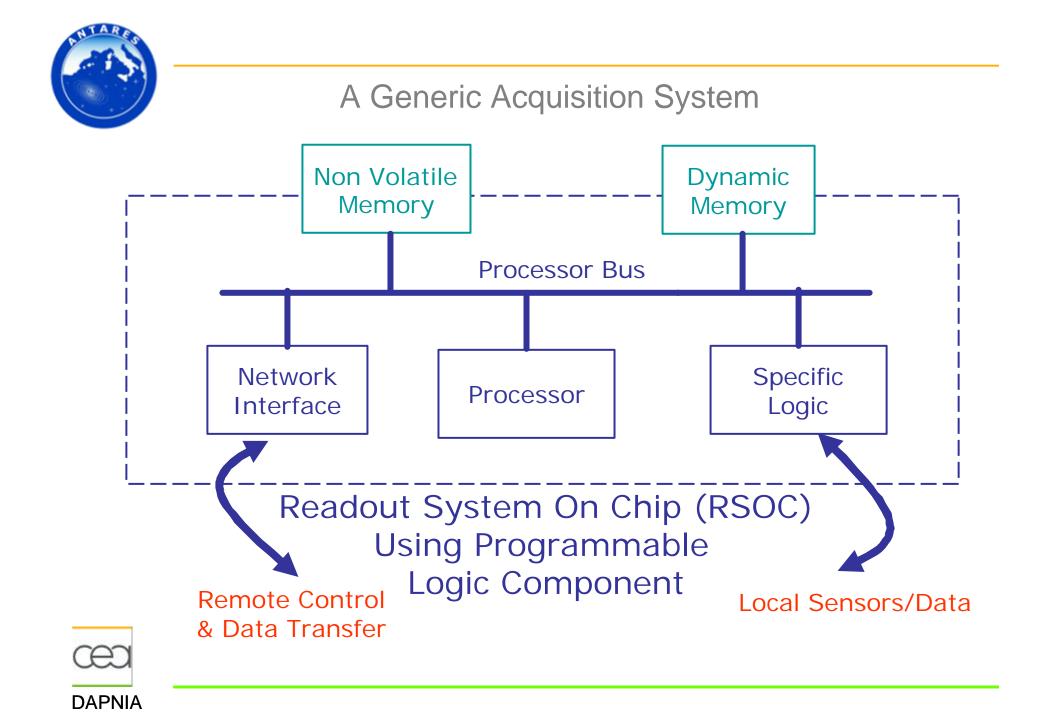
# **Readout System On Chip**

A highly integrated system using FPGA COTS

S. Anvar, <u>H. Le Provost</u>, F. Louis, B. Vallage – CEA Saclay DAPNIA –

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#### **RSOC**: The embedded Blocks

#### Processor

• Firmware, Synthesized with logical gates 32 bit RISC@150 MHz, 125 D-MIPS •Hardware, Pre-Implemented in silicon 32 bit RISC@400 MHz, 600 D-MIPS

Network Interface

Hardware

High speed serial links, Gbit Ethernet

• IP (Intellectual Property) Cores Ethernet MAC layer

#### Non Volatile Dynamic Memory Memory **Processor Bus** Network **Specific** Processor Interface Logic System On chip **Remote Control** Local Sensors

& Data Transfer

Specific logic

• Described by the user in VHDL or Verilog language

#### **Memories**

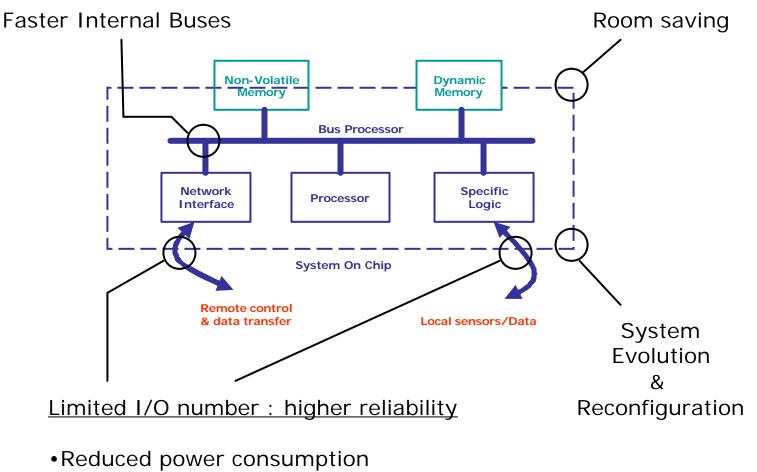
- Non-volatile: processor boot
- •Volatile: programmes & Operating System execution, data buffers



DAPNIA

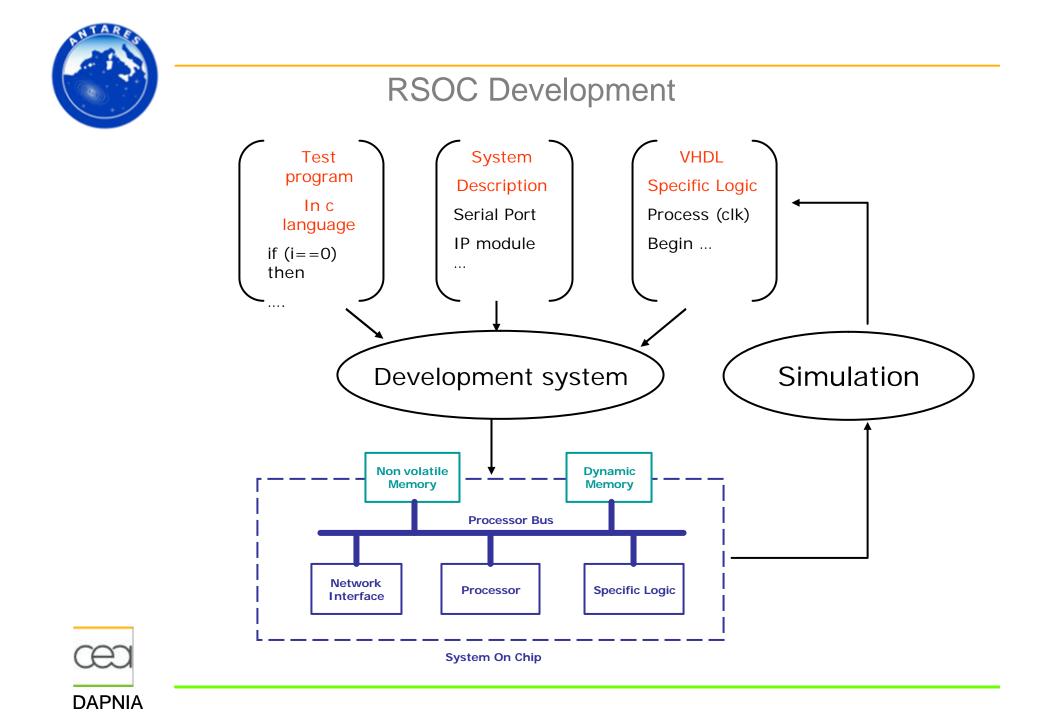


#### **RSOC** : Technical Advantages



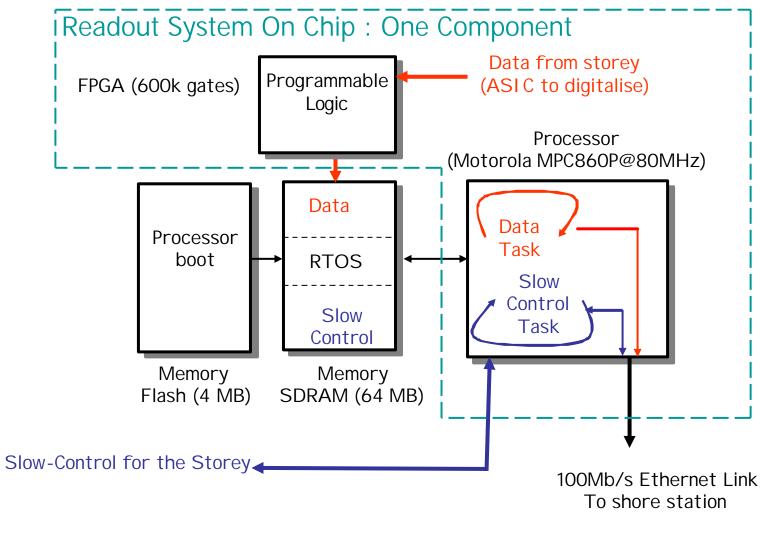
- •Less Solder faults
- •Simplified PCB



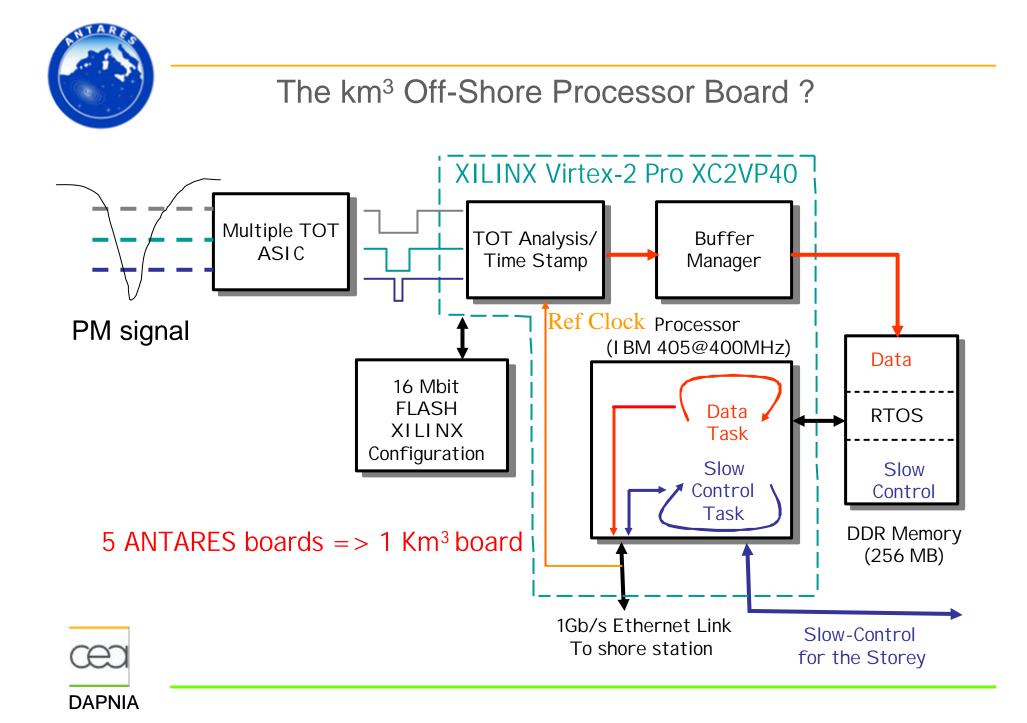




#### The ANTARES Off-Shore Processor Board



DAPNIA



AN TARES

RSOC Development programme (1)

## Generic Acquisition system

- Credit Card Format
- XILINX Virtex-2 Pro
- Memories : DDR RAM, FLASH
- I/O connector
- Ethernet ports 100 Mbit/s, 1 GBbit/s
- Operating system : vxWorks, Linux





# ANTARES Off-Shore processor board upgrade

- Hardware compatible : 100 Mbit/s port, +5V powered
- Firmware : processor interface to modify
- Software compatible : vxWorks RTOS
- Cooling system to redesign, should be simpler
- A prototype could be tested on the first deployed ANTARES String



AREA ----

# A Km<sup>3</sup> prototype

- Clock extraction and frame synchronisation (over Ethernet) to study
- Evaluate the network and CPU performances versus the power consumption
- Emulate the front end multiple TOT ASIC
- Check if a TOT ASIC is suitable for track reconstruction





### Conclusion

- ANTARES like design but with a much higher integration level
- Digital solutions, hardware and software, off-the-shelf
- Design may migrate toward a mixed Analog/Digital ASIC
- First Step for a Km3 prototype : 1 man, 1 year. Budget to buy IP, components, build a prototype

