Read Out and Data Transmission Working Group

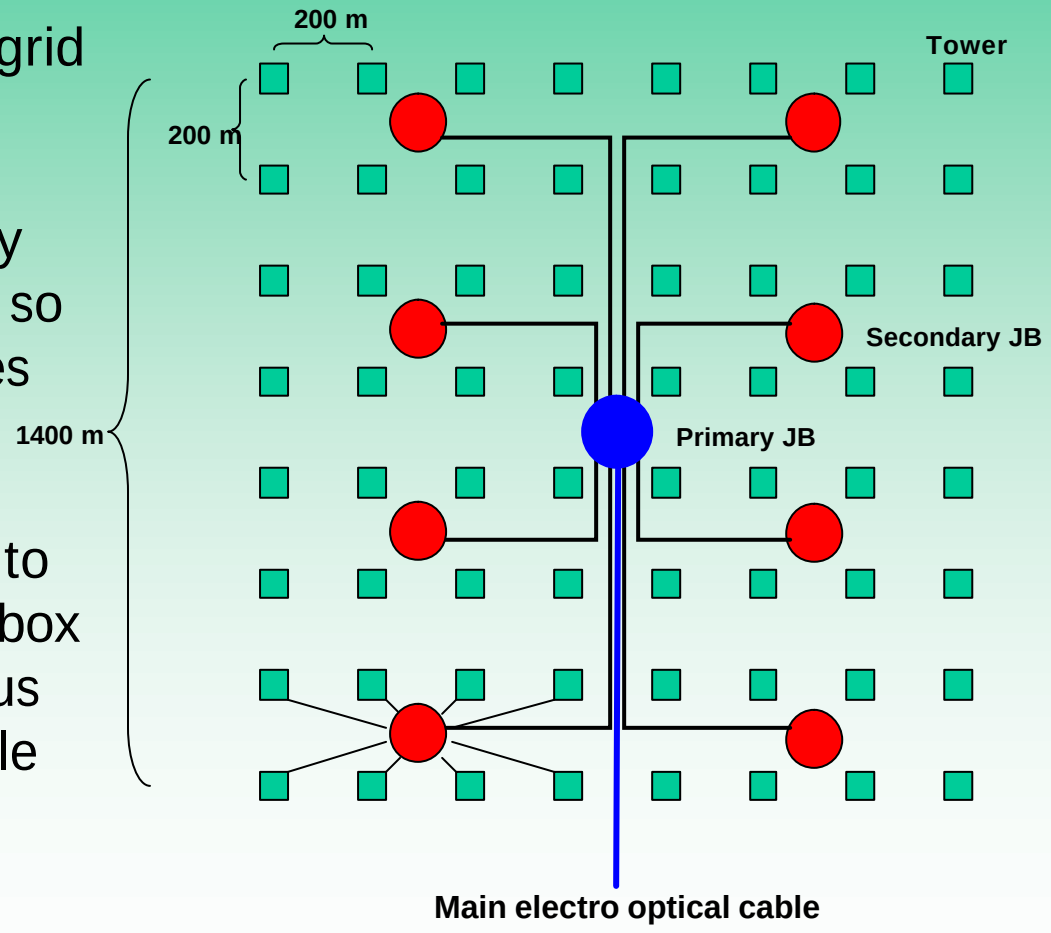
A 200-MHz FPGA based PMT acquisition electronics for NEMO experiment

The NEMO Km3 experiment

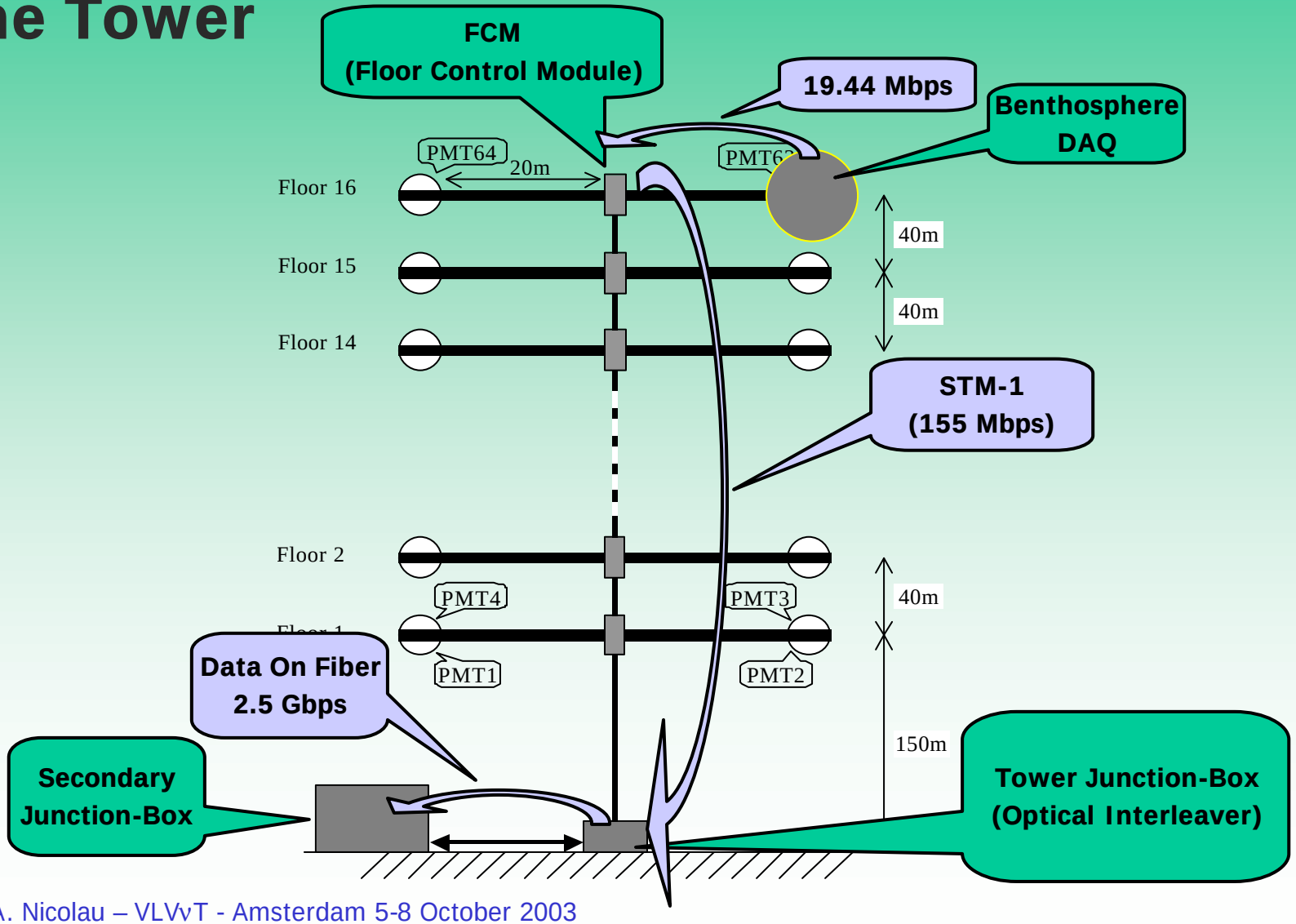
64 towers placed on a square grid (8x8).

The towers are electro-optically linked (8 by 8) to one of the 8 so called secondary junction boxes (S-JB).

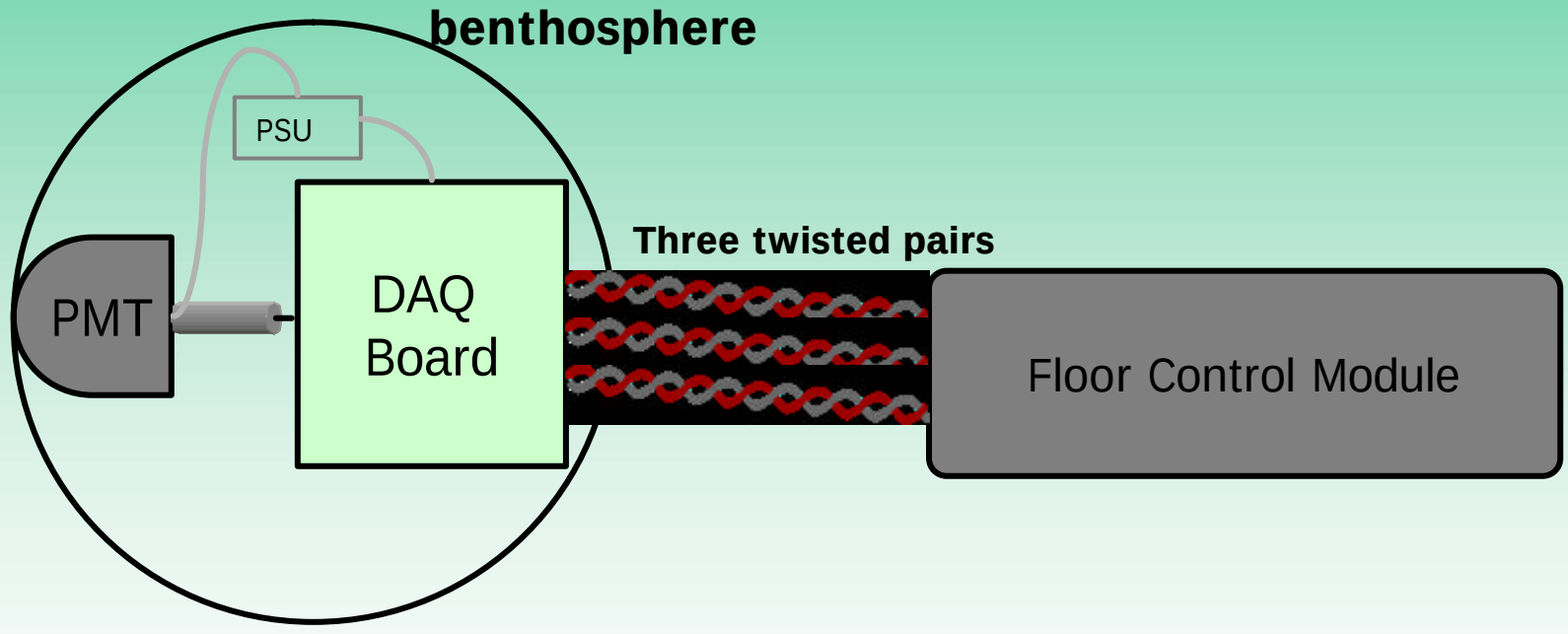
The S-JBs are then connected to the so called primary junction box (P-JB) which links the apparatus to the main electro-optical cable arriving from on shore.



The Tower


FCM
(Floor Control Module)
19.44 Mbps
Benthosphere
DAQ
PMT64
20m
PMT62
Floor 16
Floor 15
Floor 14
40m
40m
STM-1
(155 Mbps)
Floor 2
PMT4
PMT3
40m
PMT1
PMT2
Data On Fiber
2.5 Gbps
150m
Secondary
Junction-Box
Tower Junction-Box
(Optical Interleaver)

Data acquisition electronics



Constraints

PMT Signal:
Bandwidth **100MHz**
Output voltage range: **0 ¸ -40V**
Threshold value for L0 trigger: ~ -**30mV** (~1/4 photoelectron for 13" PMT)

Single photoelectron rate (due to ^{40}K):
Event rate (with a 13" PMT): ~**50 kevents/s**
Event length: ~**50ns**

Electro-mechanical:
Power consumption as low as possible (long distance power transport).
Long *mean time between failure* (no repairing possible).
Small & simple (the fewer the components the more reliable the system).

Constraints: consequences

PMT Signal Bandwidth: 100MHz

Sampling rate: 200MHz

PMT Signal Dynamics: -40V / -30mV ~ 1300 → 2048 (11 bit)

Sampling resolution: 8 bit
Quasi logarithmic analog compression

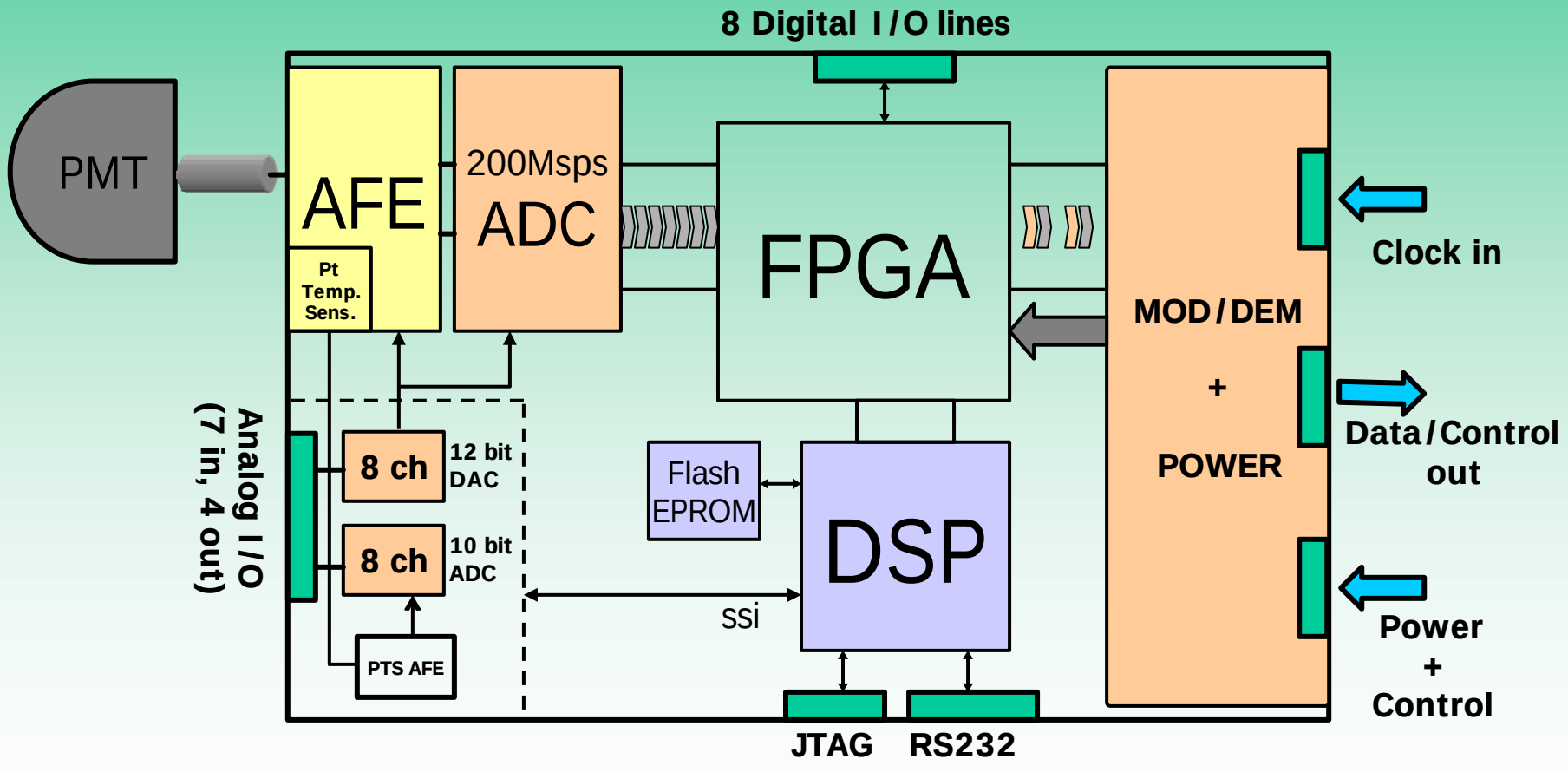
DAQ Input Signal Dynamics: -40V / -18mV

Physical data rate (for a 13" PMT):
50 kevents/s X (100 bit/event) ~ **5Mbps**

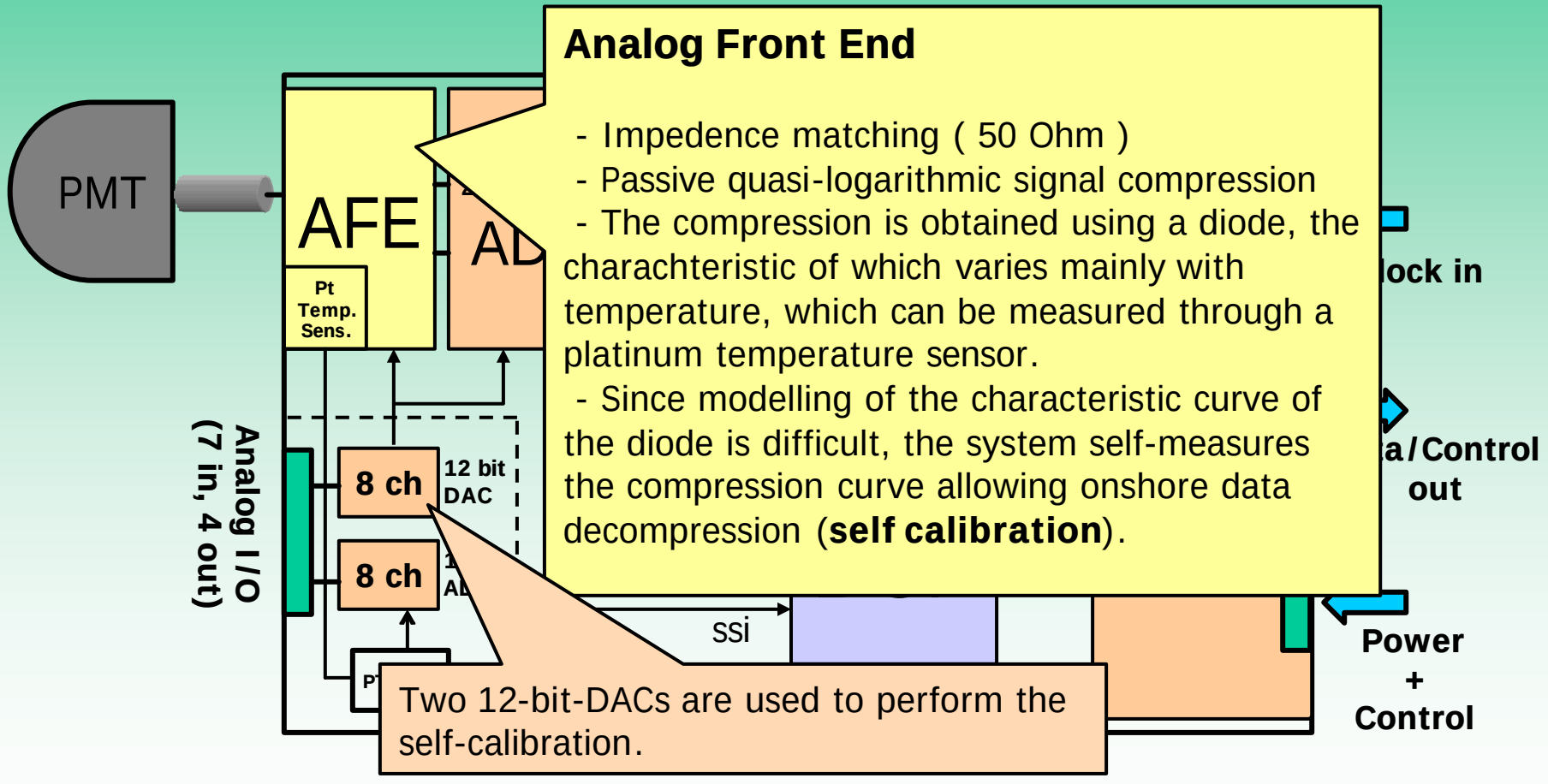
Sampling data rate: 200MHz X 8bit = 1.6Gbps

Thus, using a **user definable digital threshold**, the sampling data rate can be reduced to the expected value of 5Mbps.

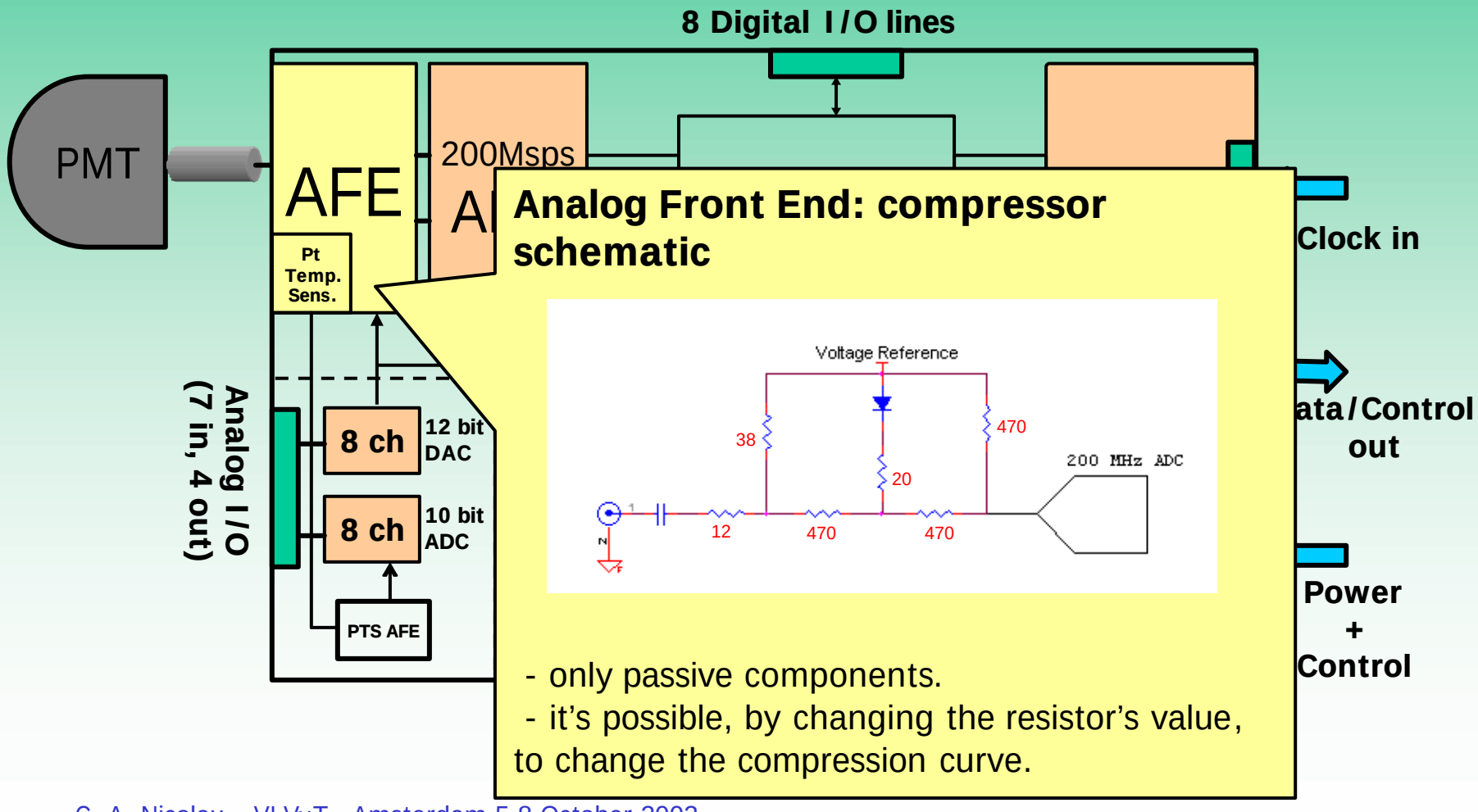
Block diagram



The Analog Front End



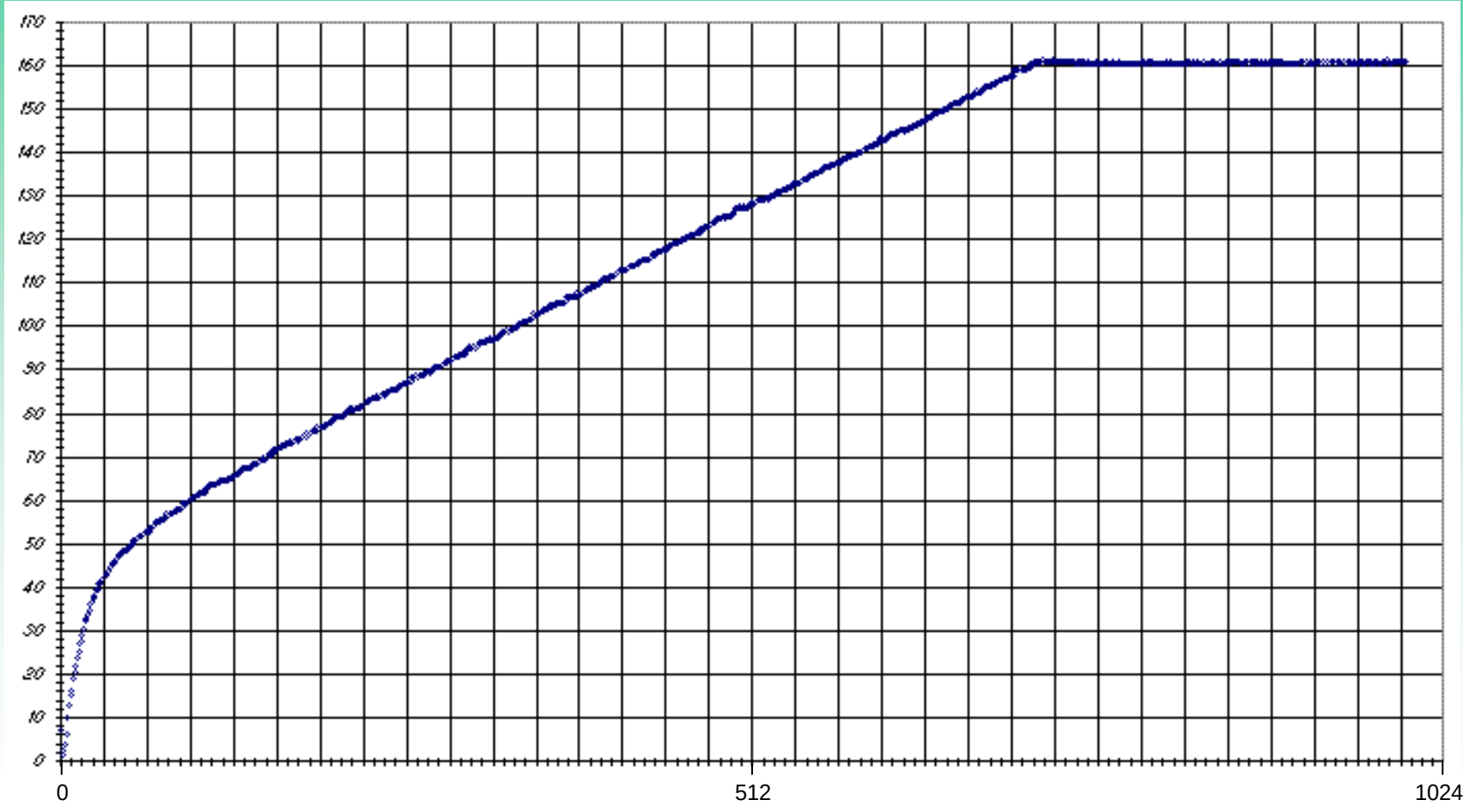
The Analog Front End



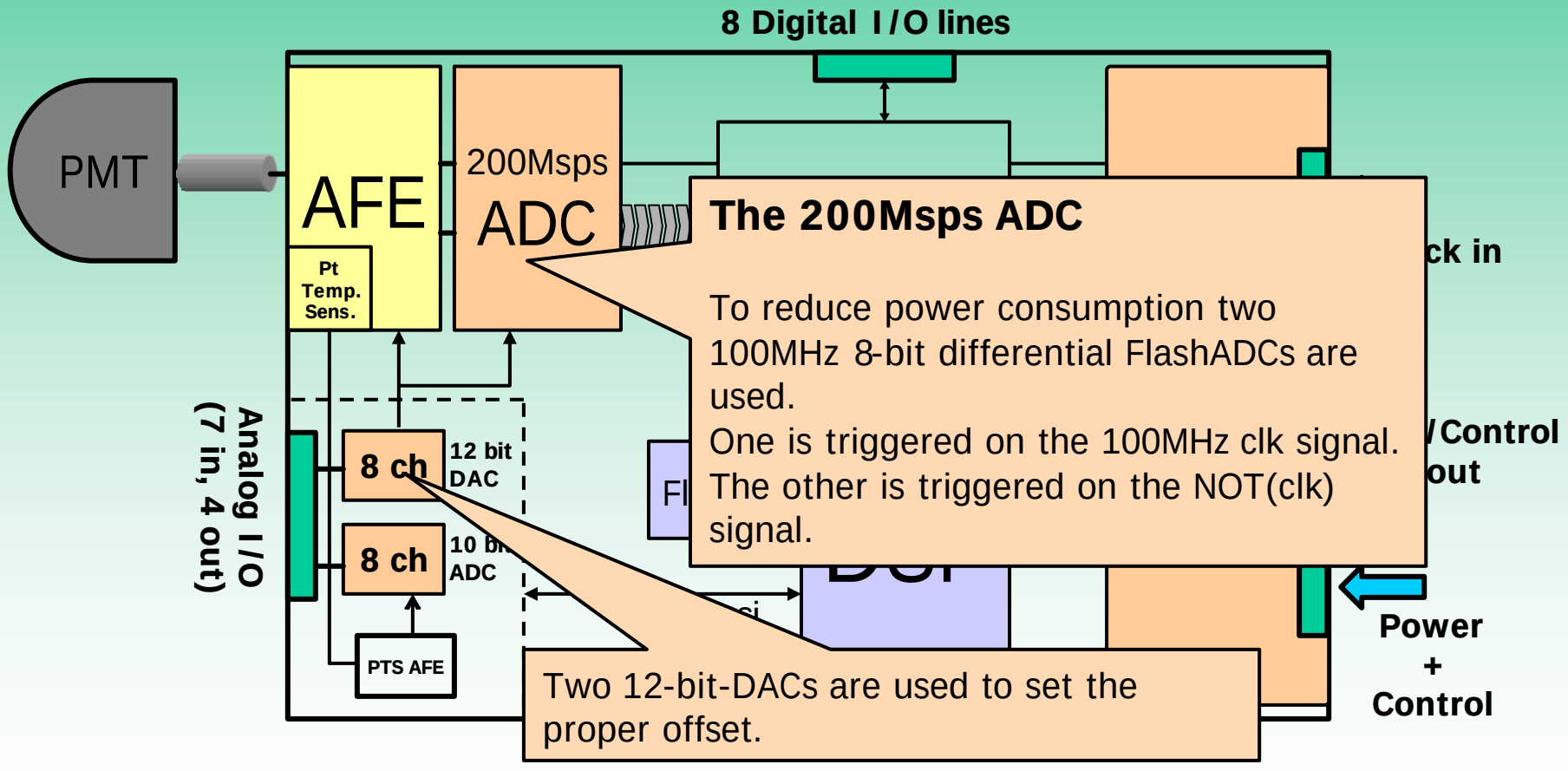
Analog Front End: compressor schematic

- only passive components.
- it's possible, by changing the resistor's value, to change the compression curve.

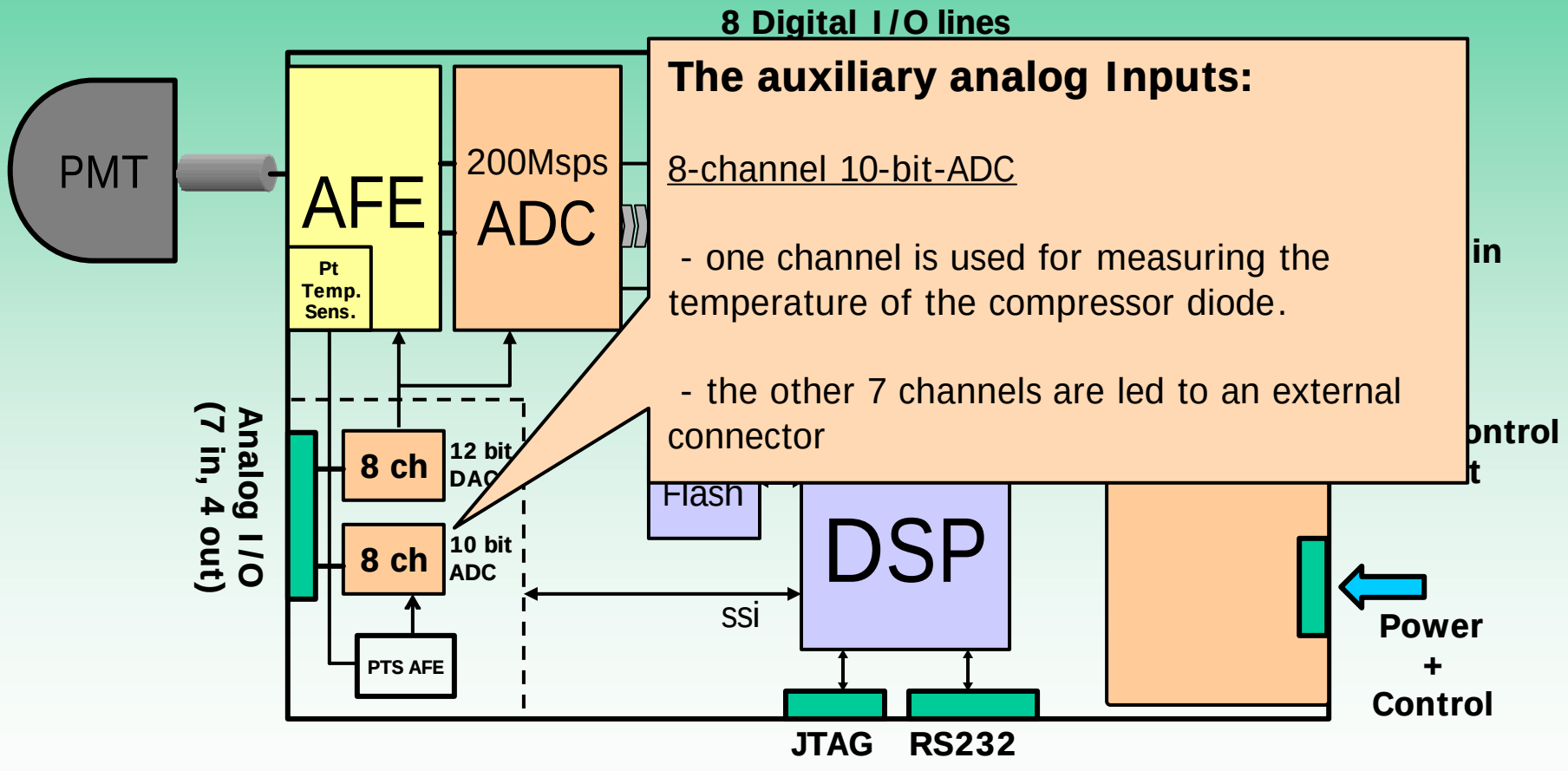
The Analog Front End: calibration curve



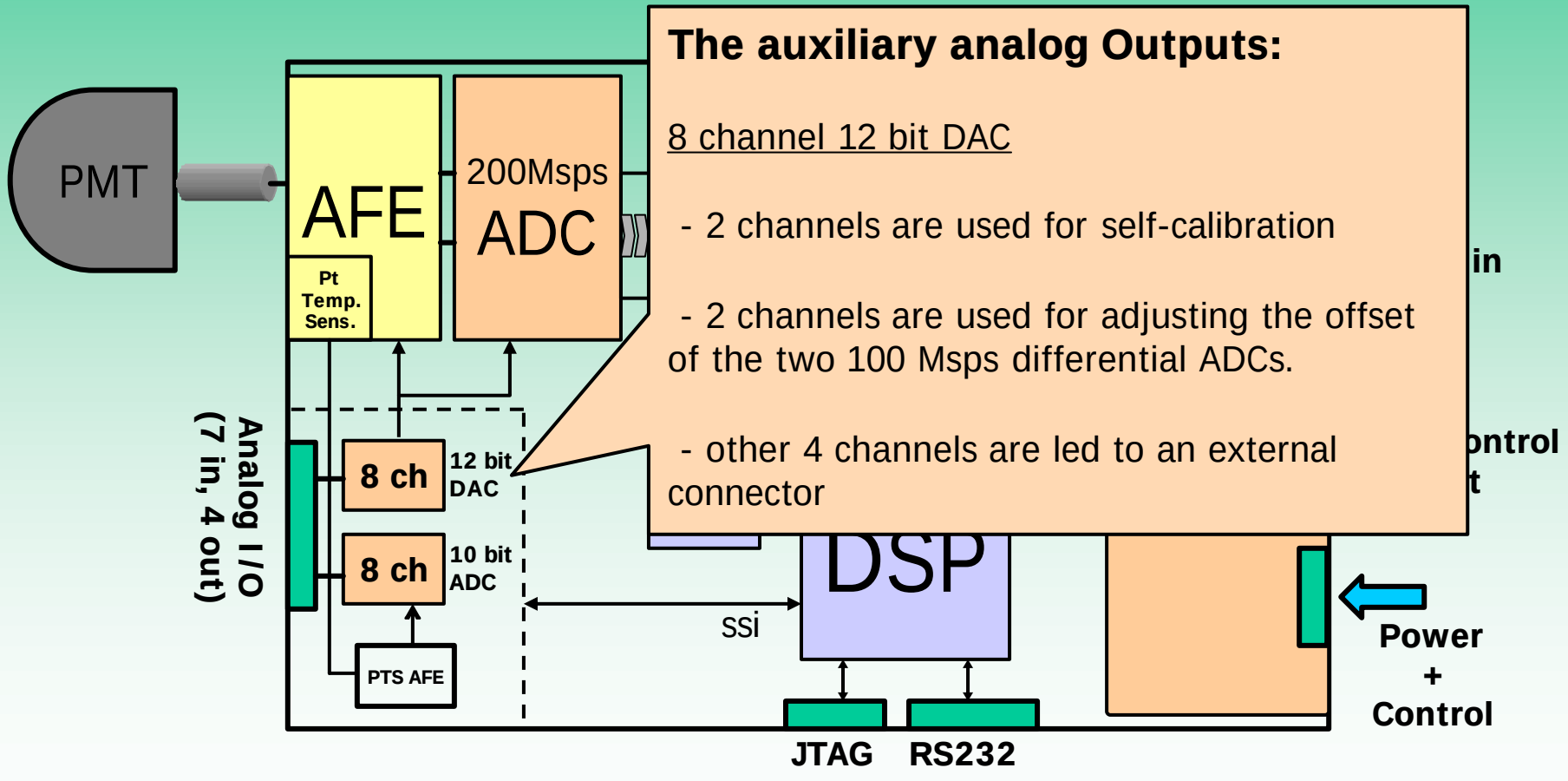
200 Msample/s analog to digital conversion



The Auxiliary analog I/Os



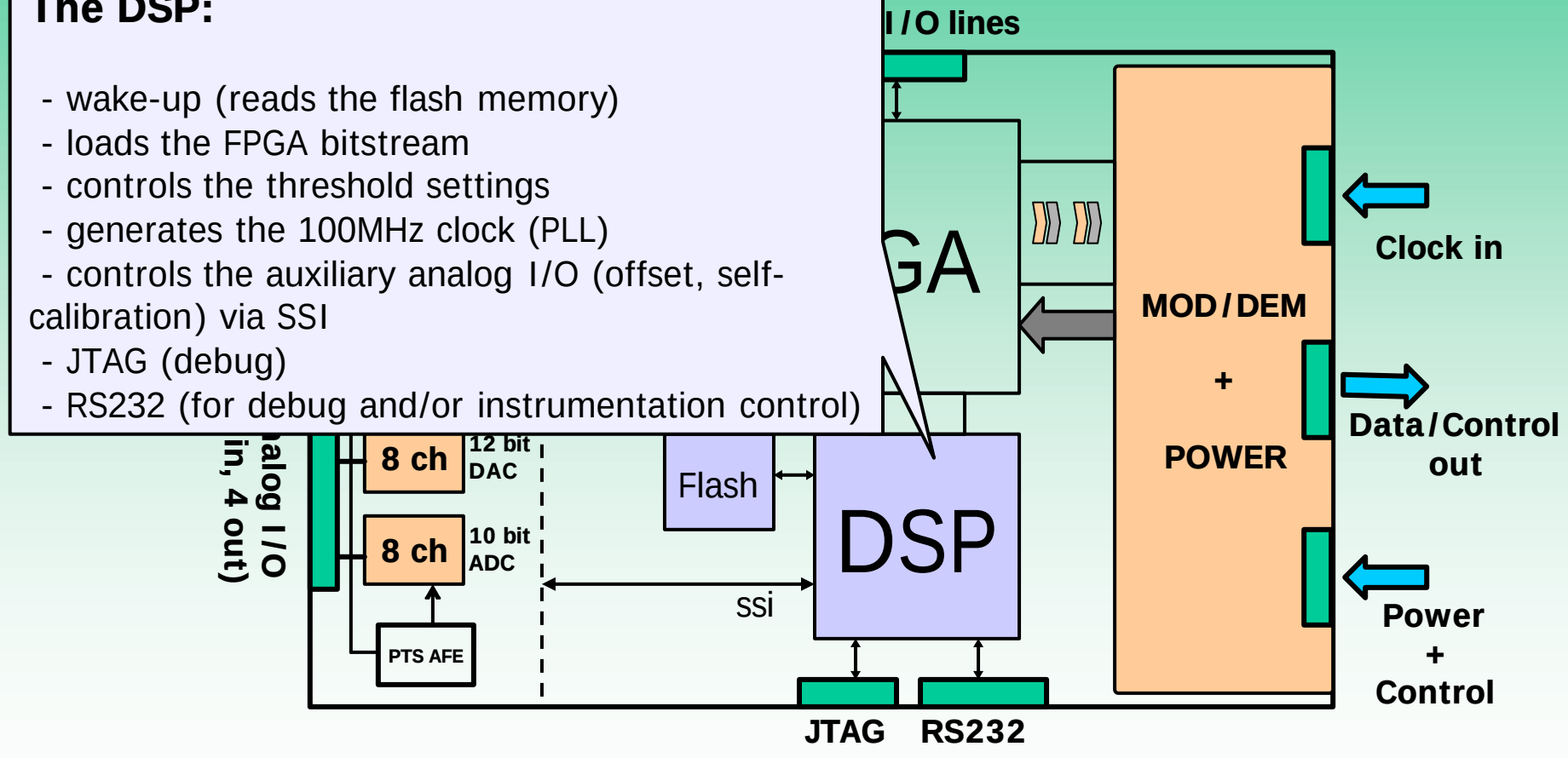
The Auxiliary analog I/Os



The DSP

The DSP:

- wake-up (reads the flash memory)
- loads the FPGA bitstream
- controls the threshold settings
- generates the 100MHz clock (PLL)
- controls the auxiliary analog I/O (offset, self-calibration) via SSI
- JTAG (debug)
- RS232 (for debug and/or instrumentation control)



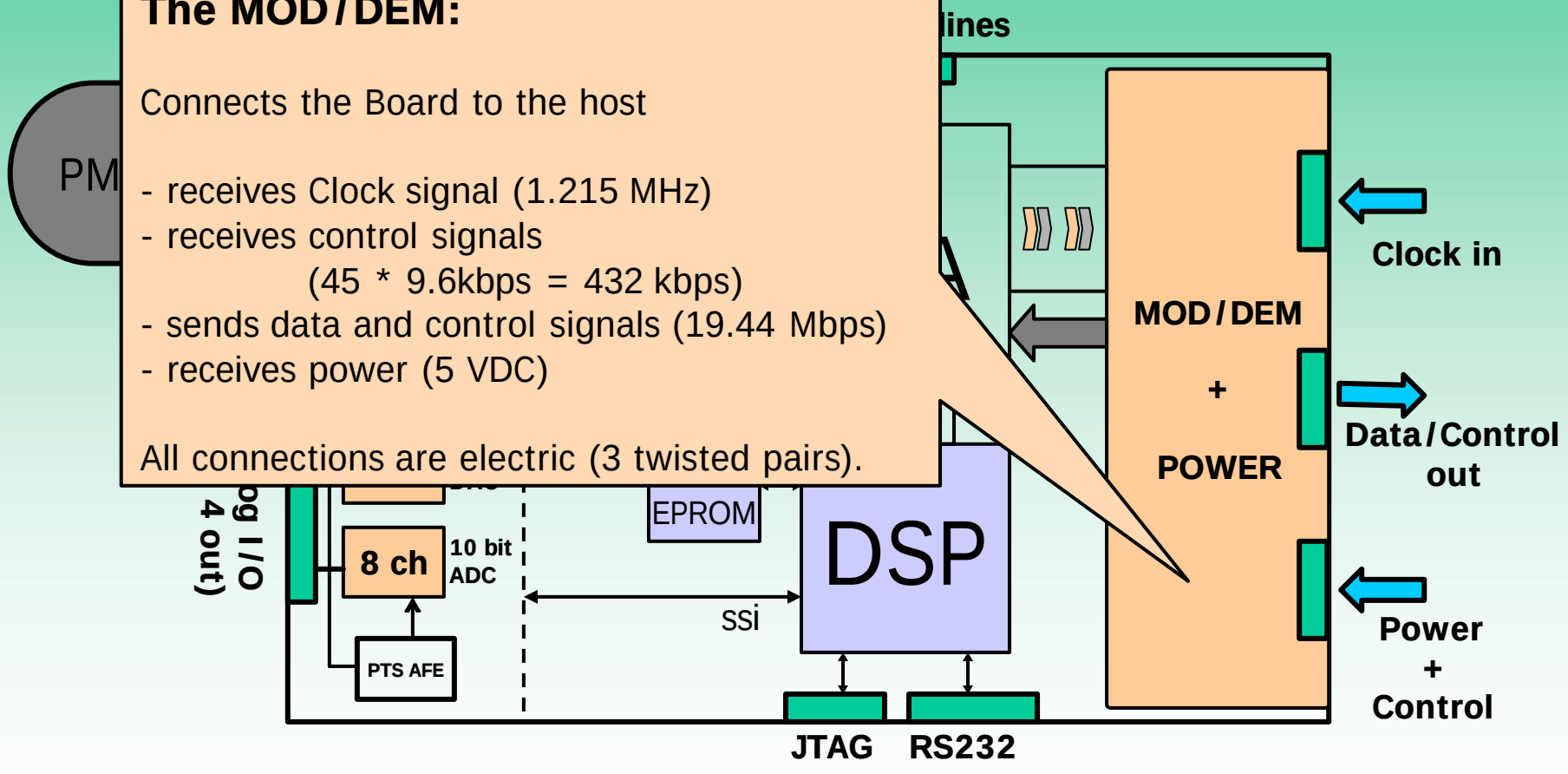
The MOD/DEM block

The MOD/DEM:

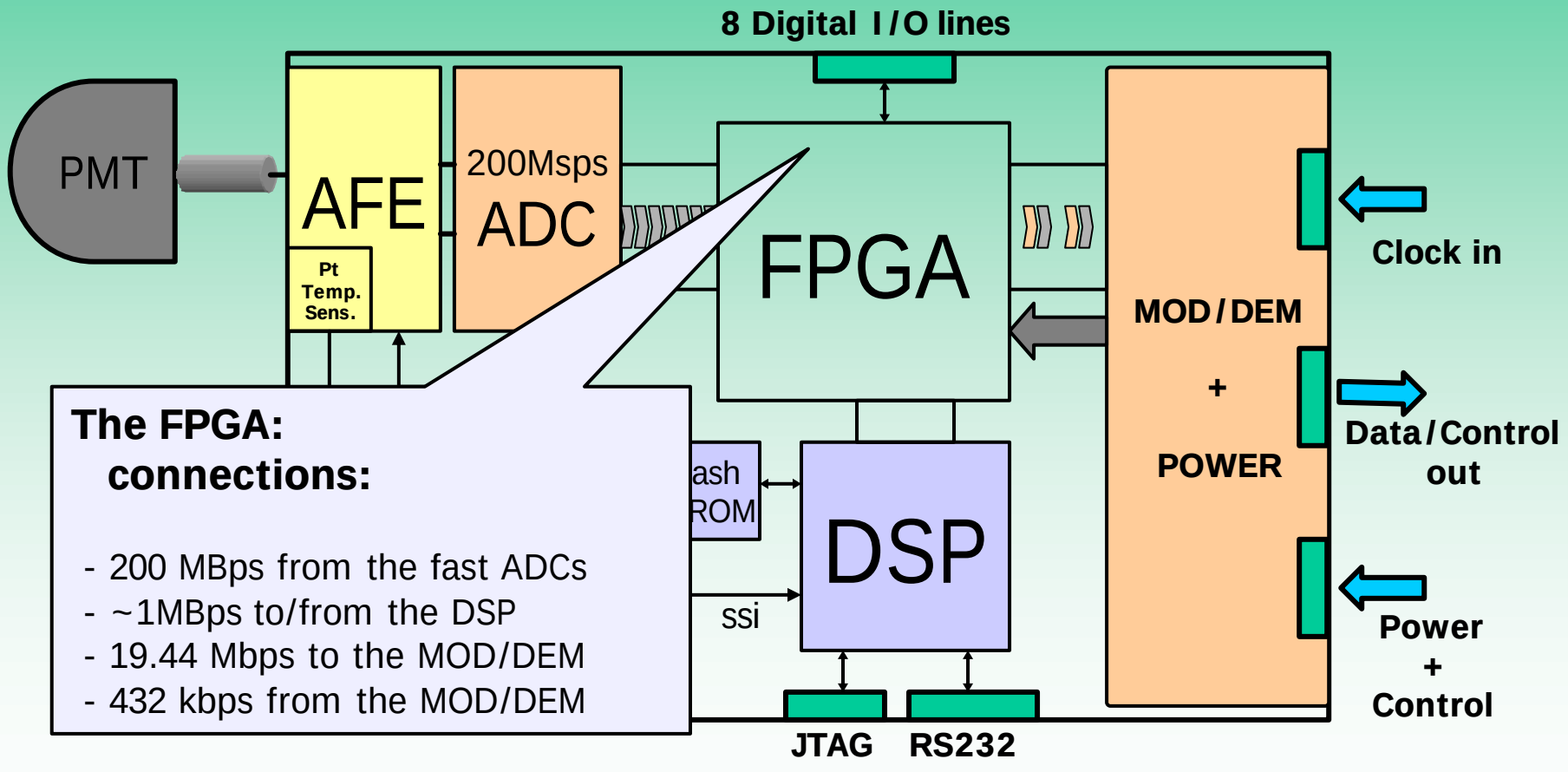
Connects the Board to the host

- receives Clock signal (1.215 MHz)
- receives control signals
  (45 * 9.6kbps = 432 kbps)
- sends data and control signals (19.44 Mbps)
- receives power (5 VDC)

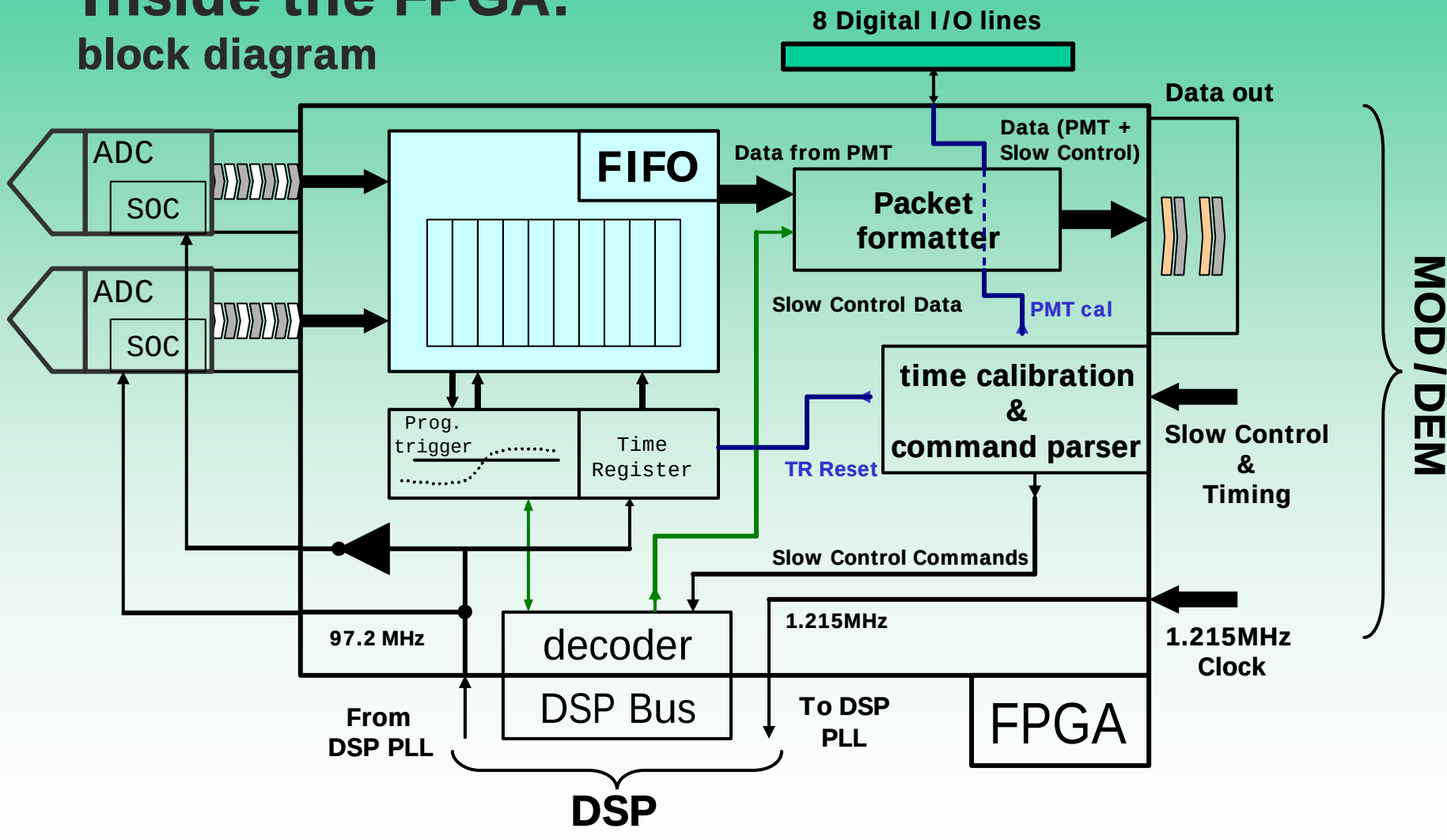
All connections are electric (3 twisted pairs).



The FPGA

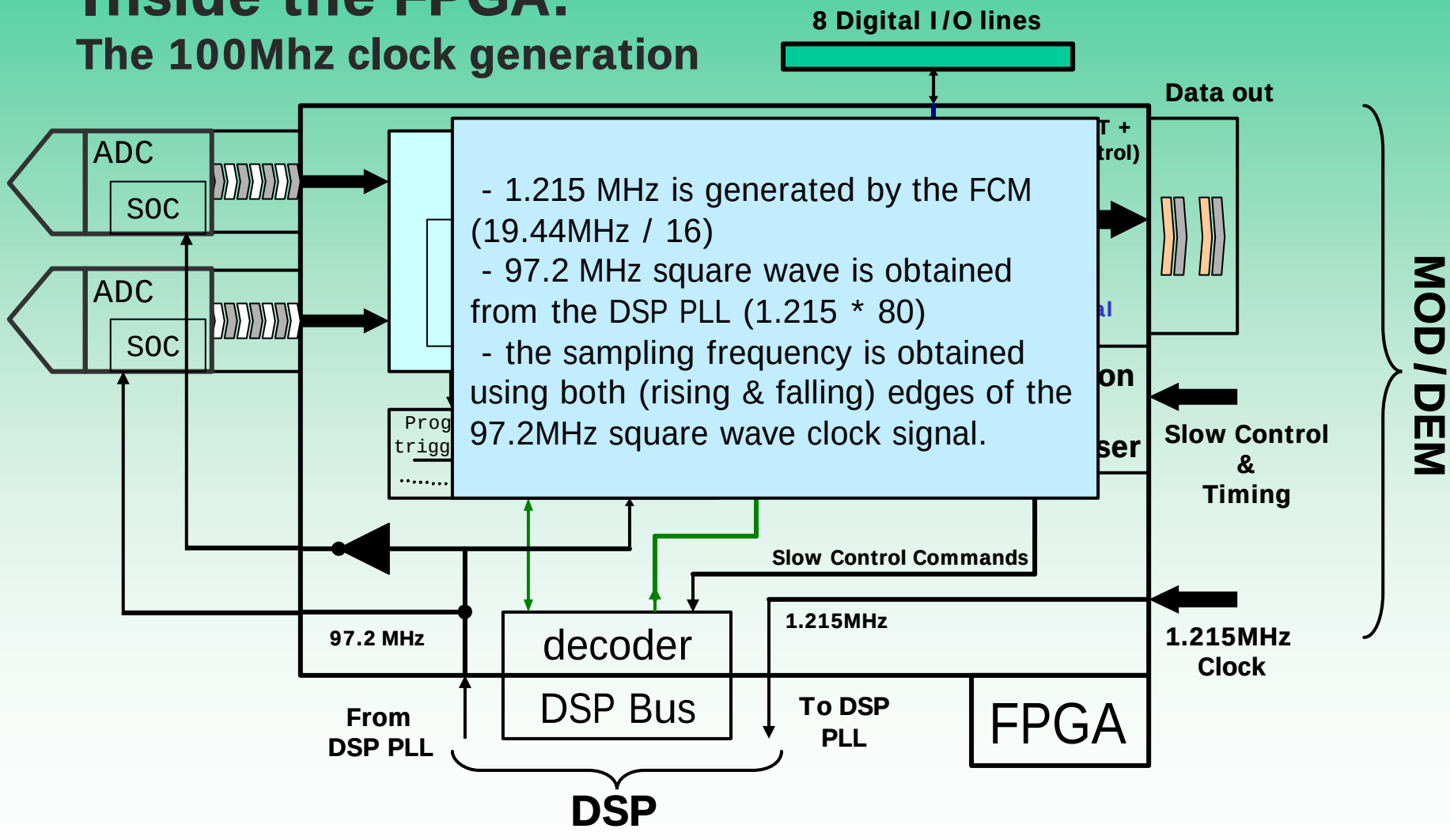

8 Digital I/O lines
PMT
AFE
Pt Temp. Sens.
200Msps ADC
FPGA
MOD/DEM + POWER
Clock in
Data/Control out
Power + Control
ash ROM
DSP
ssi
JTAG
RS232
The FPGA: connections:
- 200 MBps from the fast ADCs
- ~1MBps to/from the DSP
- 19.44 Mbps to the MOD/DEM
- 432 kbps from the MOD/DEM

Inside the FPGA:
block diagram



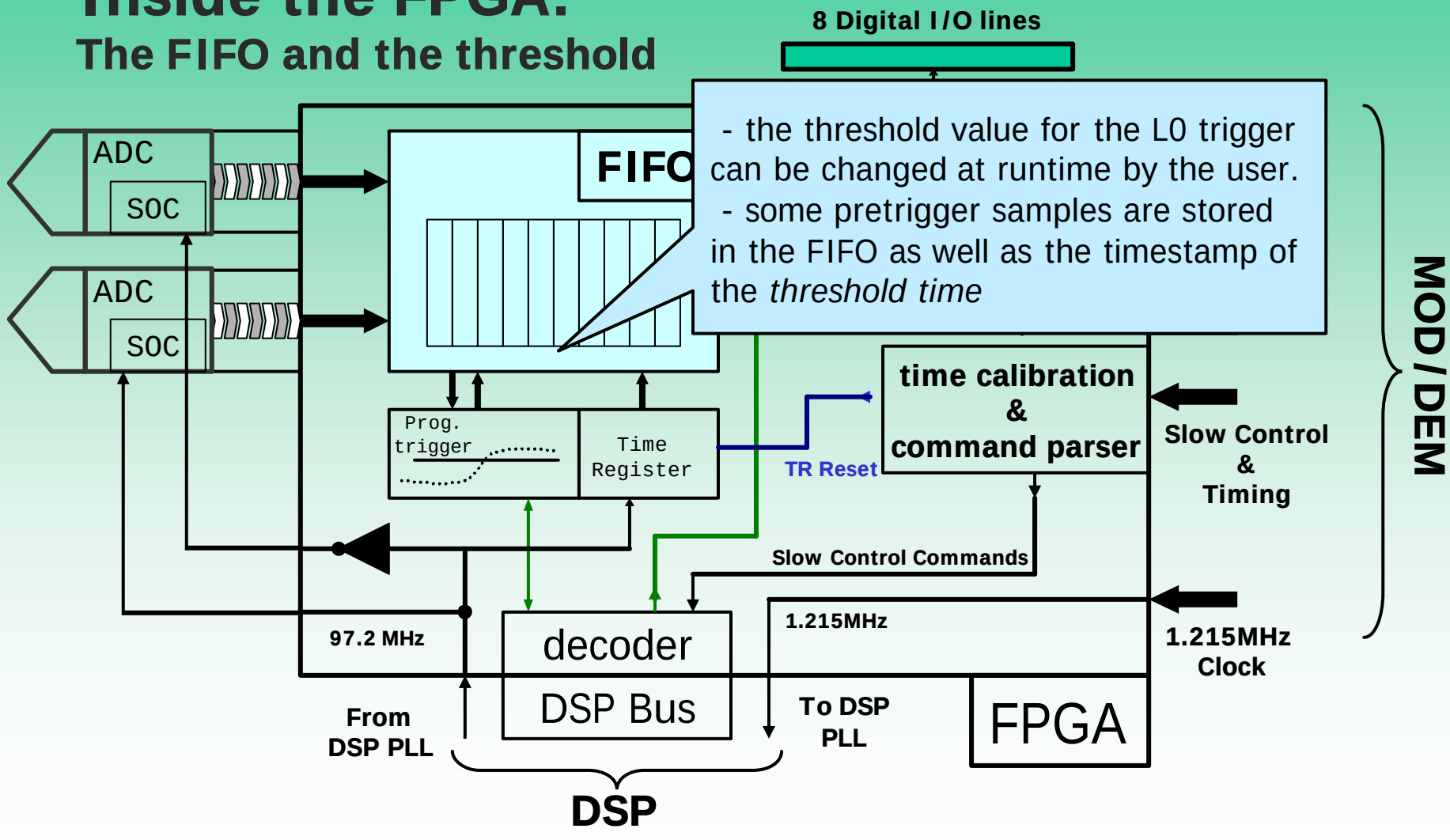
Inside the FPGA:

The 100Mhz clock generation



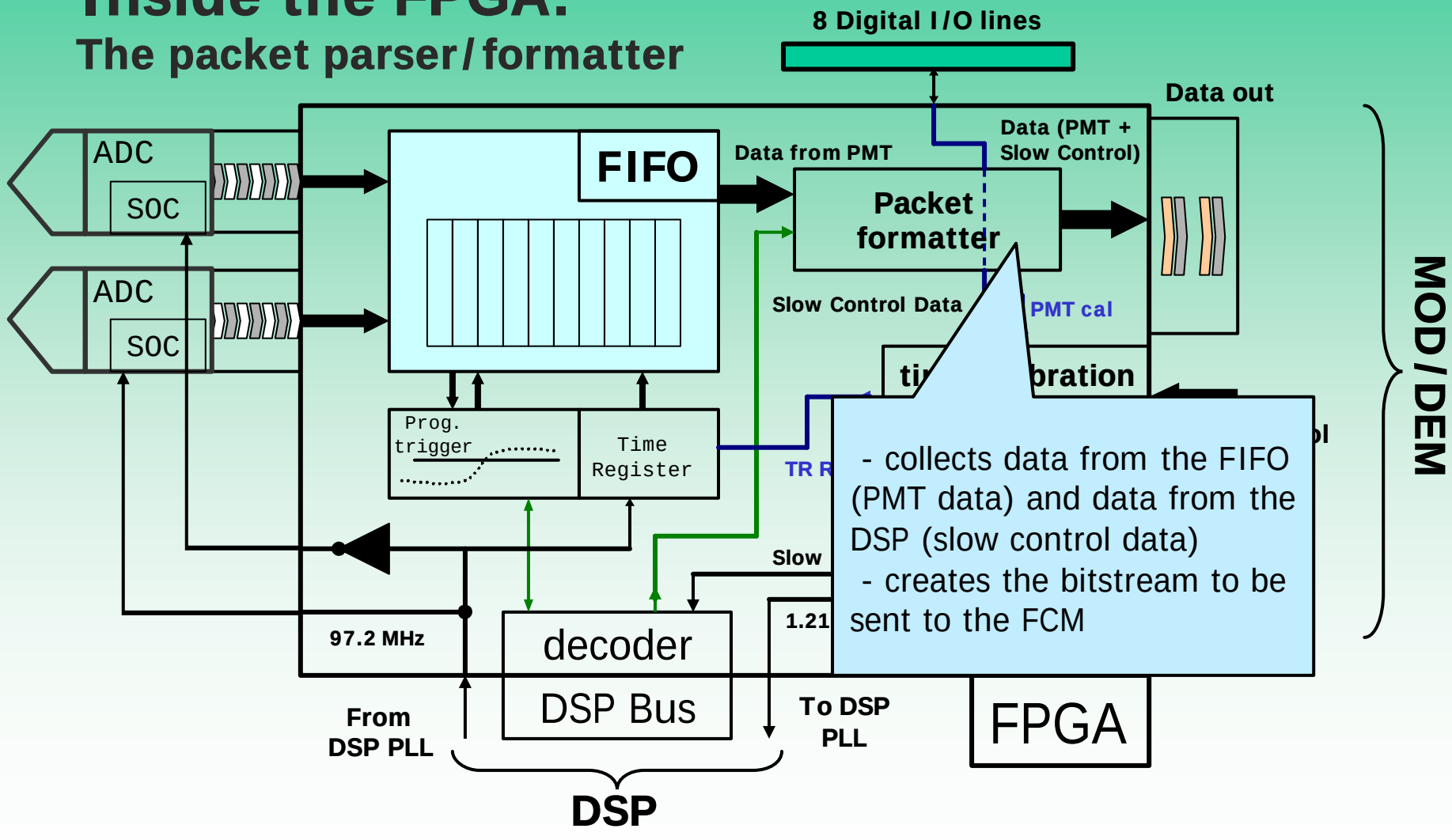
Inside the FPGA:

The FIFO and the threshold



Inside the FPGA:

The packet parser/formatter



Inside the FPGA:

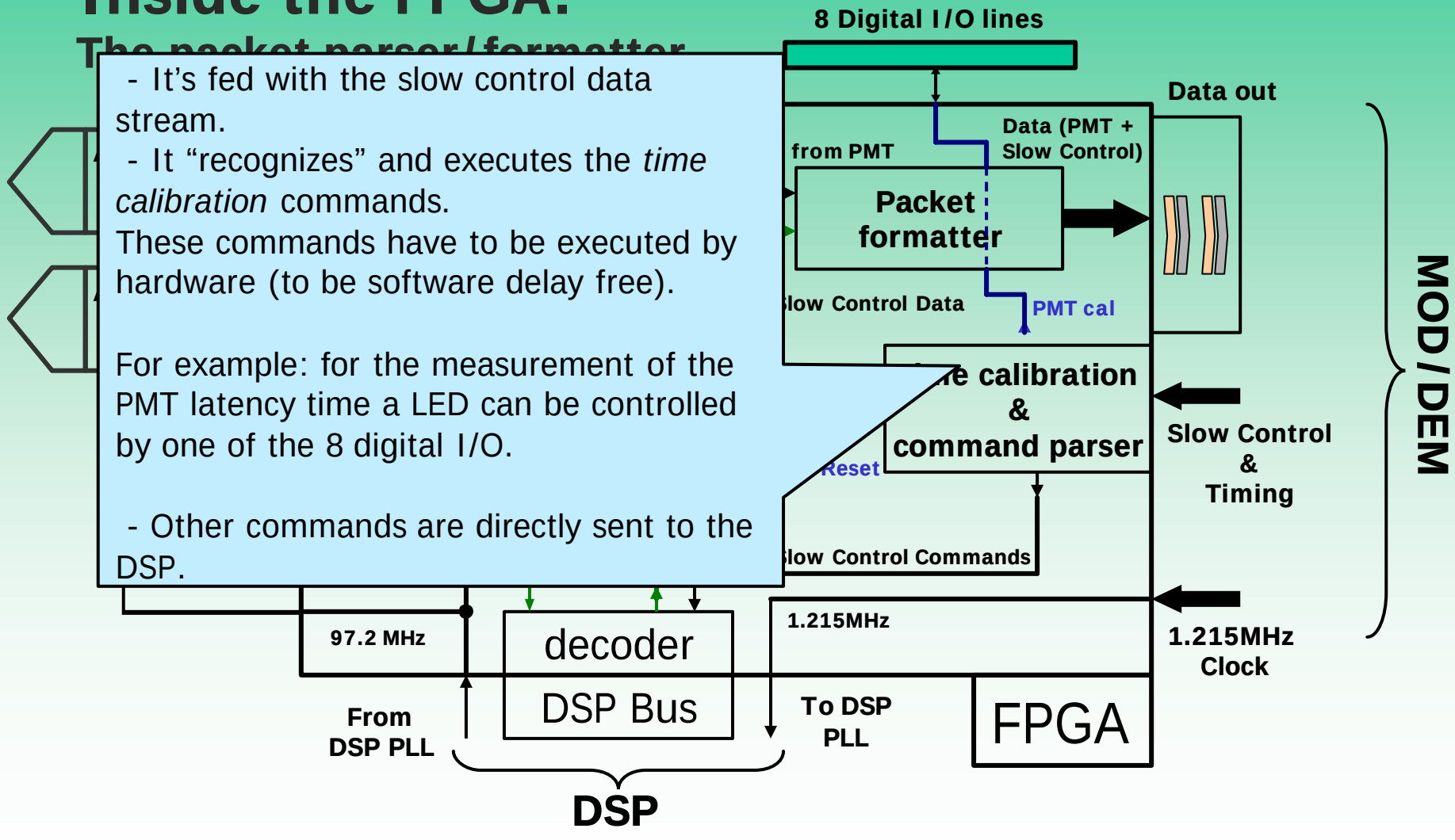
The packet parser/formatter

- It's fed with the slow control data stream.
- It "recognizes" and executes the *time calibration* commands.

These commands have to be executed by hardware (to be software delay free).

For example: for the measurement of the PMT latency time a LED can be controlled by one of the 8 digital I/O.

- Other commands are directly sent to the DSP.



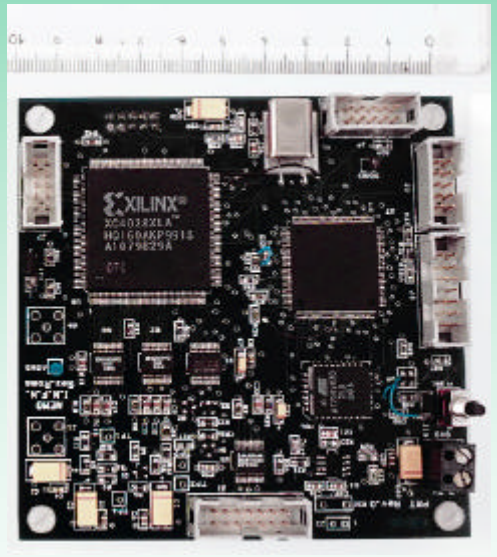
The protoype

Characteristics:

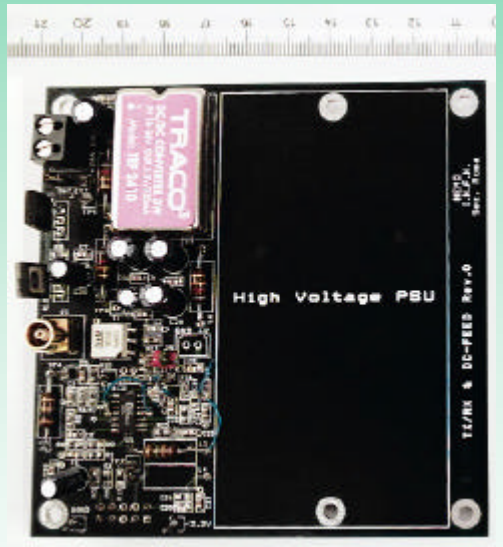
FPGA: Xilinx XC4028XLA
DSP: Motorola DSP56303
100Msps ADCs: AD9283

Physical dimensions:
2 x (10 cm) x (10 cm)

Power consumption:
~950mW



DAQ



MOD / DEM + HVPSU

Flexibility towards the Km3

- The allocated bandwidth of the output data channel is over-dimensioned compared to the physical one.
Thus, by changing the FPGA firmware, it's possible to allocate different data bandwidth.

- The number of auxiliary channels is reduntant.
Probably, for the NEMO Km3 we won't need all the 7 A/D channels, 4 D/A channels, 8 digital I/O lines, reducing number of components, power consumption, and physical dimension.

- Using newer FPGA, it's possible to **implement the DSP functions inside the FPGA**, reducing dimensions, power consumption, costs.

Goal: power consumption < 500mW